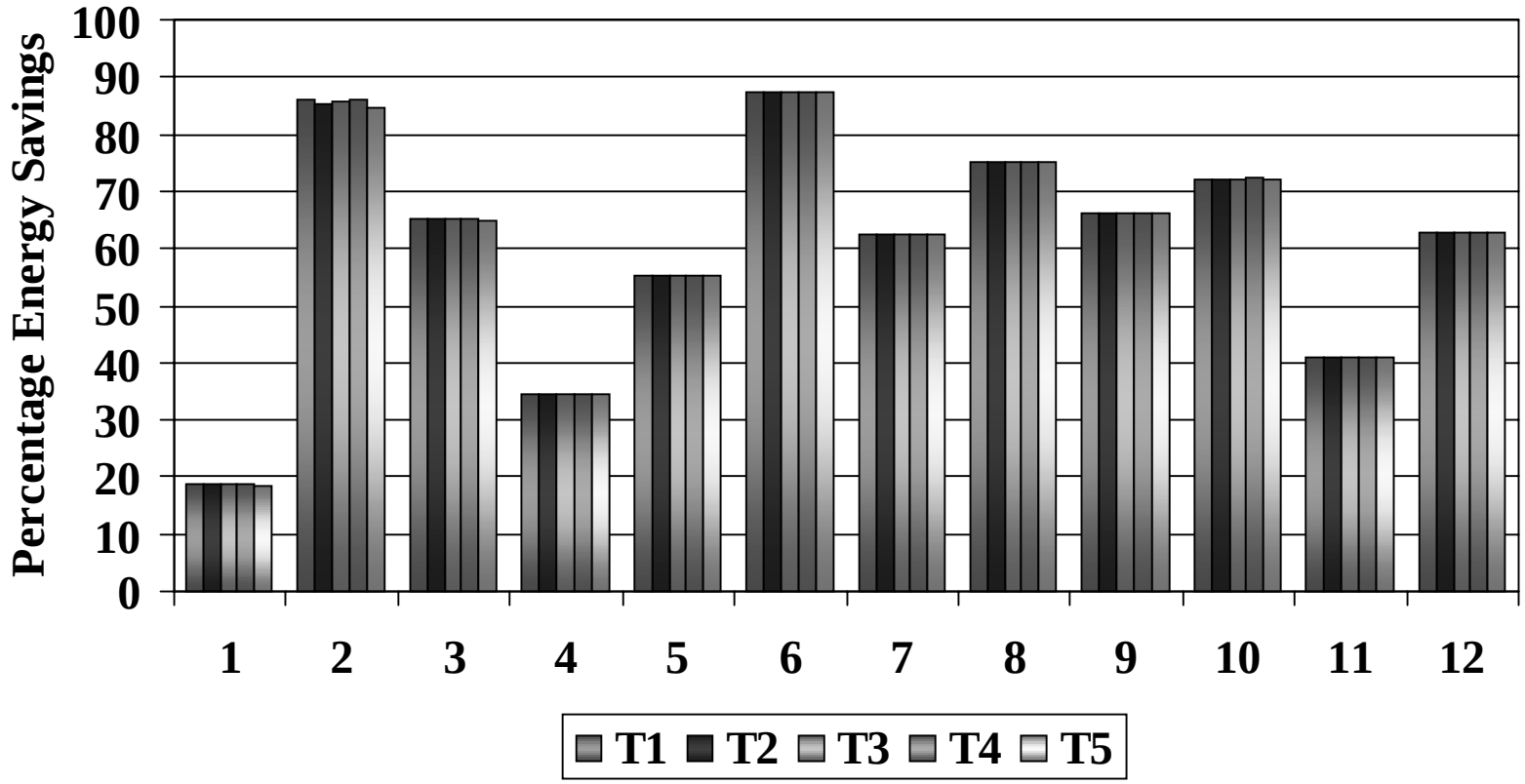
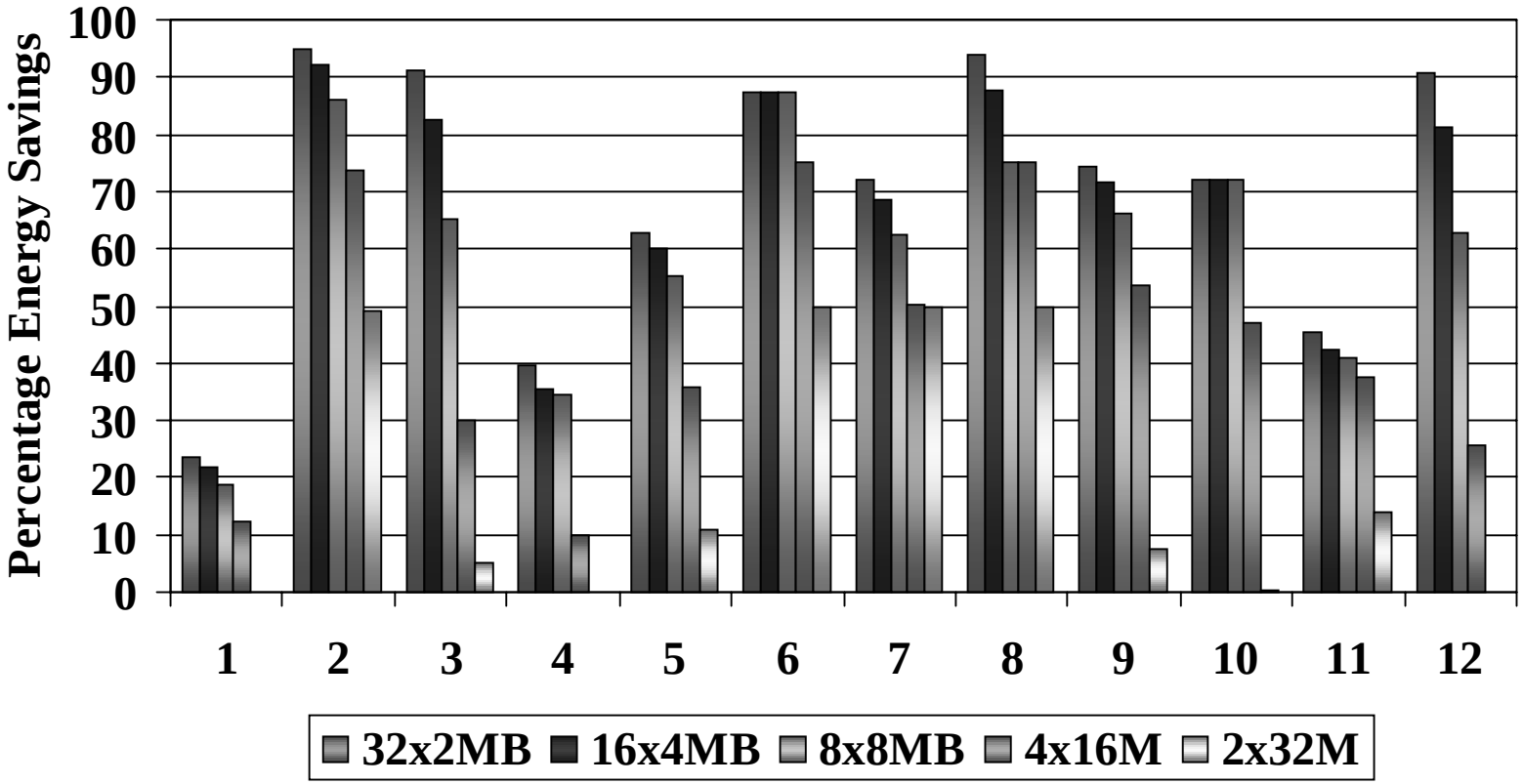
Technology Trends

- T1: Base configuration
- T2: Improved circuit technology (e.g., dual threshold voltages)
- T3: Increased leakage current with very low supply voltage
- T4: Reduced synchronization times
- T5: T2+T3+T4

Energy Savings (Technological Trends)



Energy Savings (Memory Organizations)

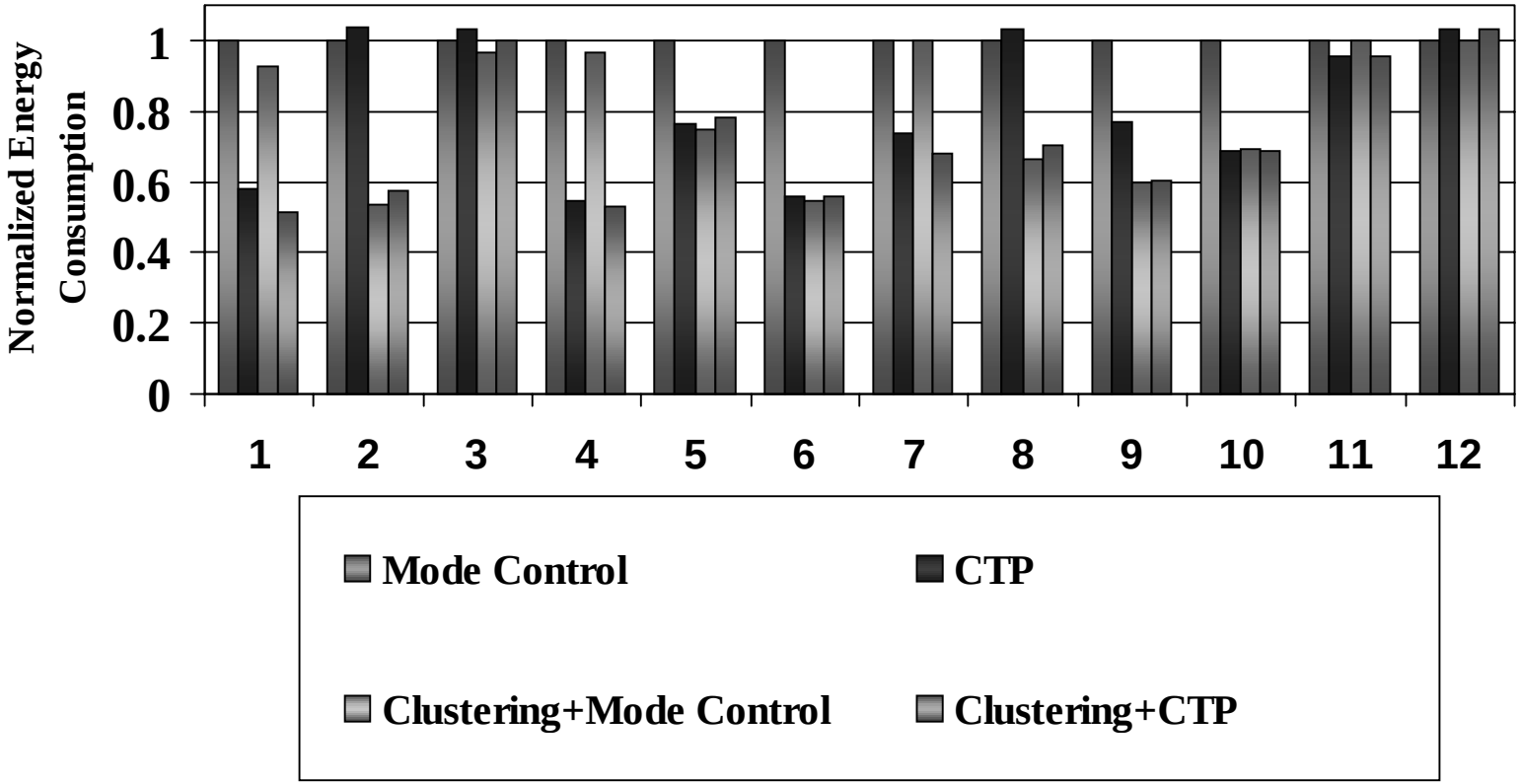


Hardware Optimizations for Partitioned Memory

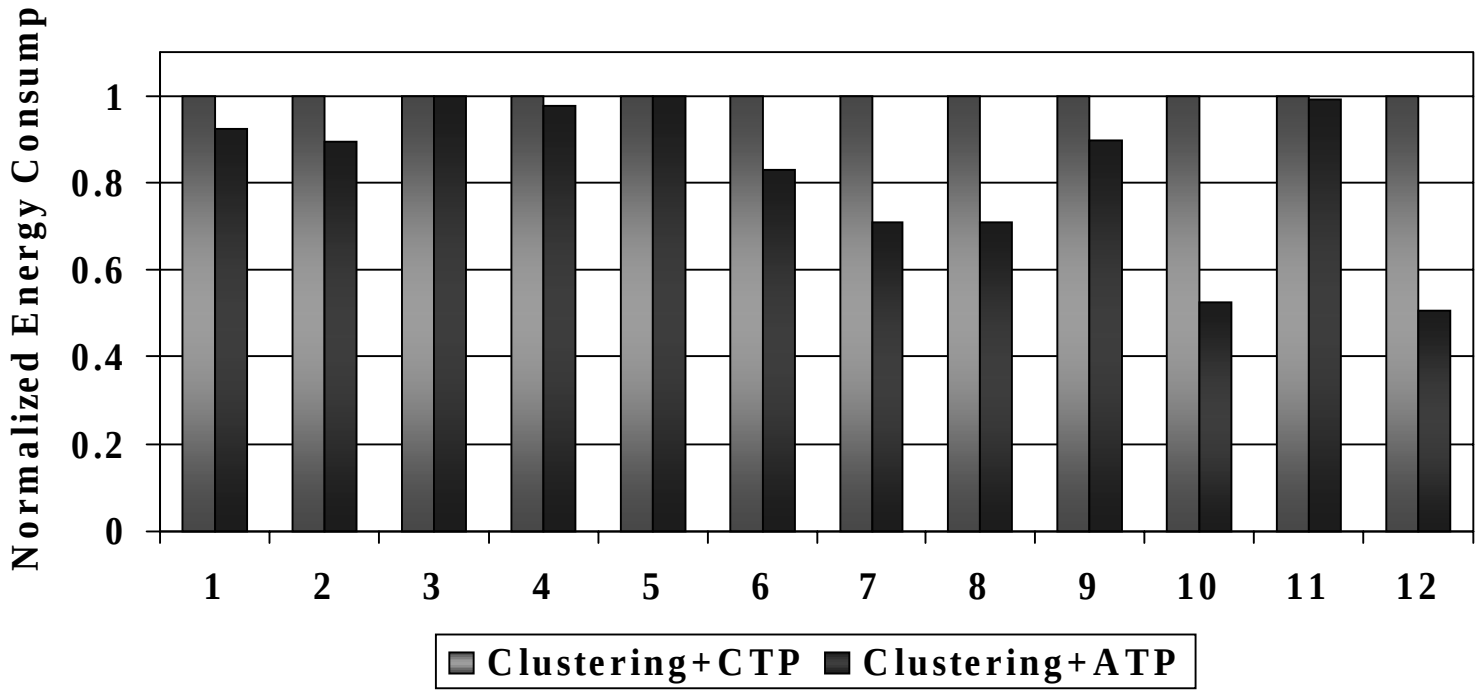
If a module not accessed in a while, it will not be accessed in the near future

- Constant Threshold Predictor (CTP)
- Adaptive Threshold Predictor (ATP)
- History-Based Predictor (HBP)

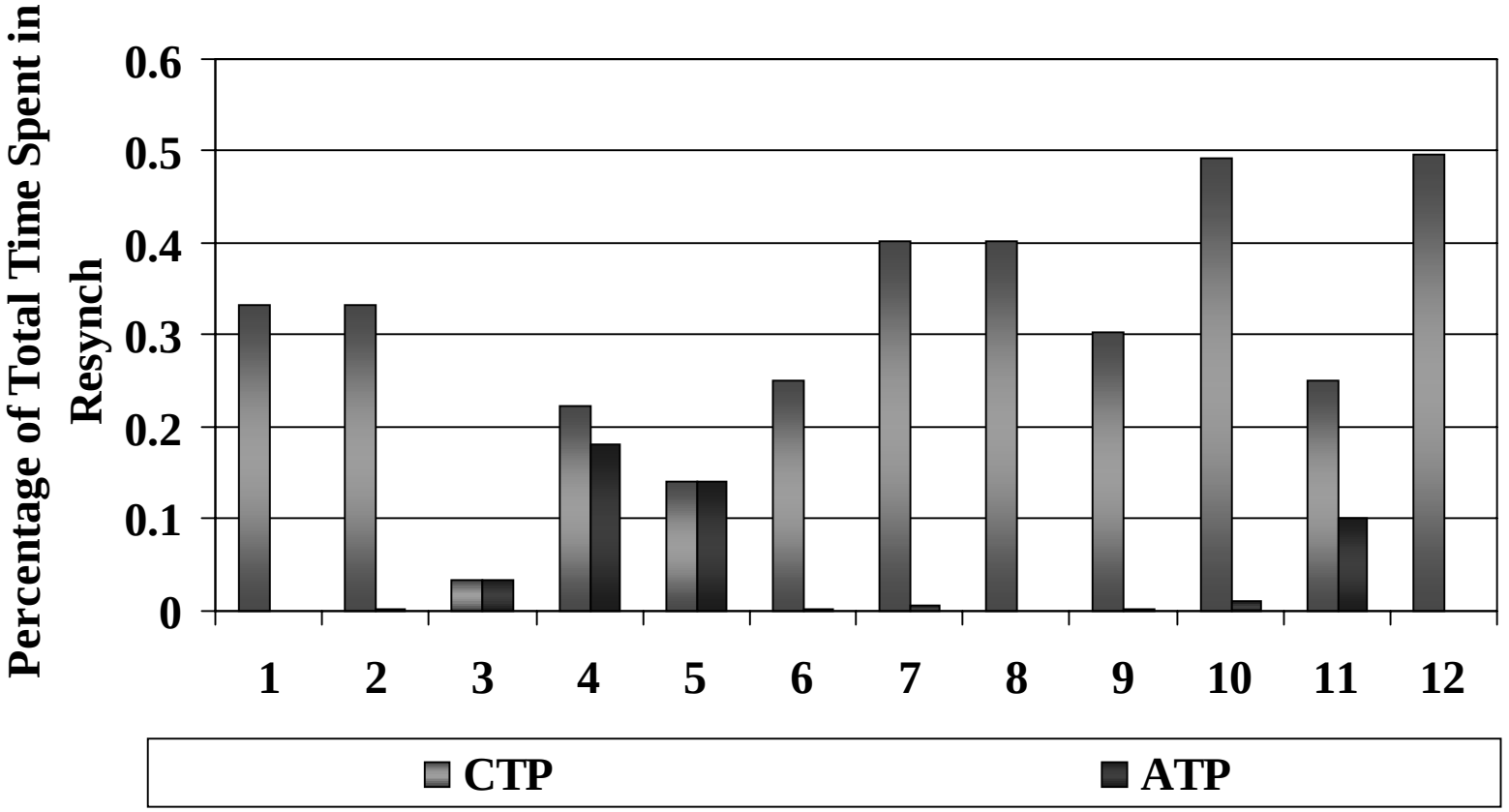
Energy Savings with CTP



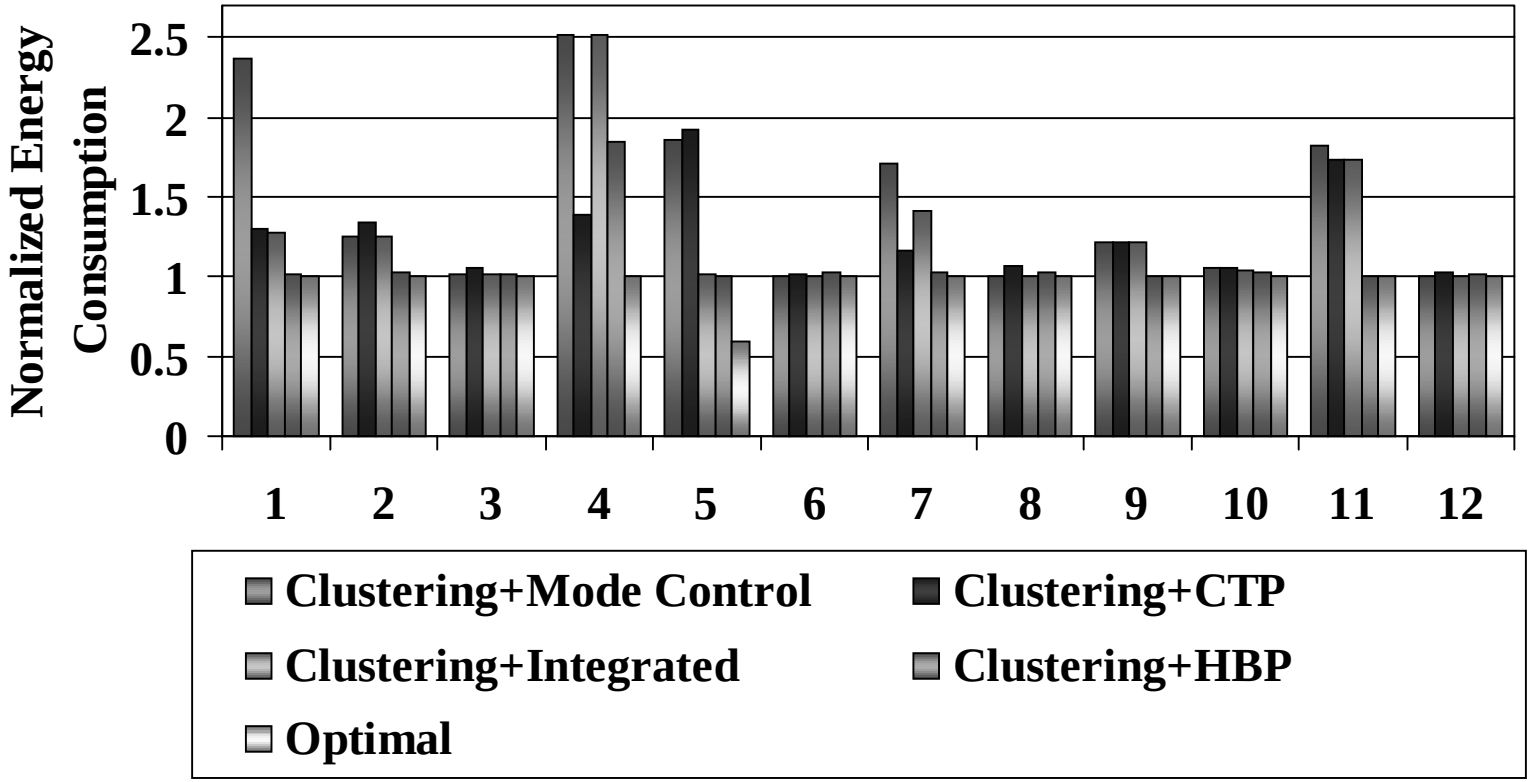
Energy Savings with ATP



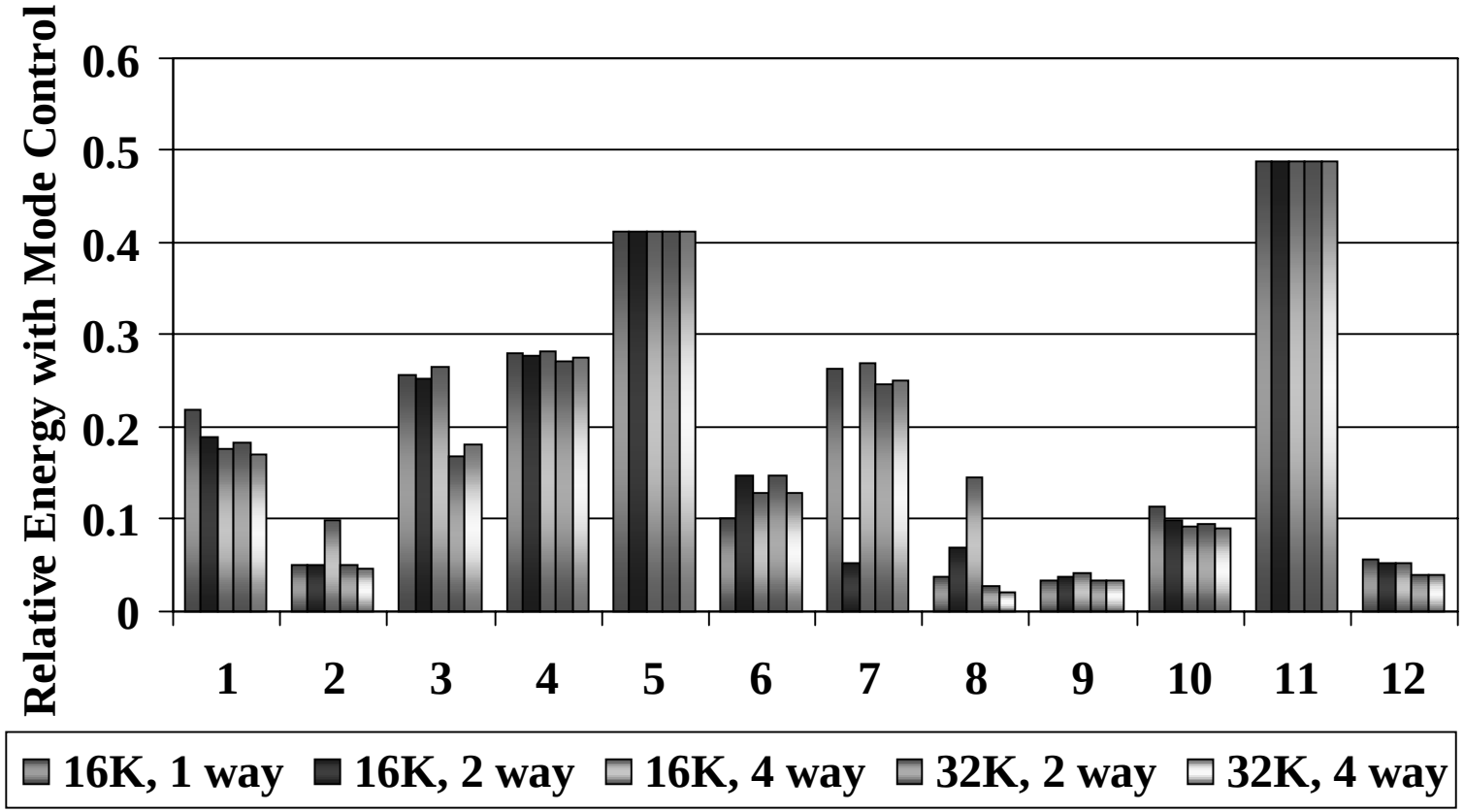
Resynchronization Times with ATP and CTP



Energy Savings



HBP with Different Cache Configurations



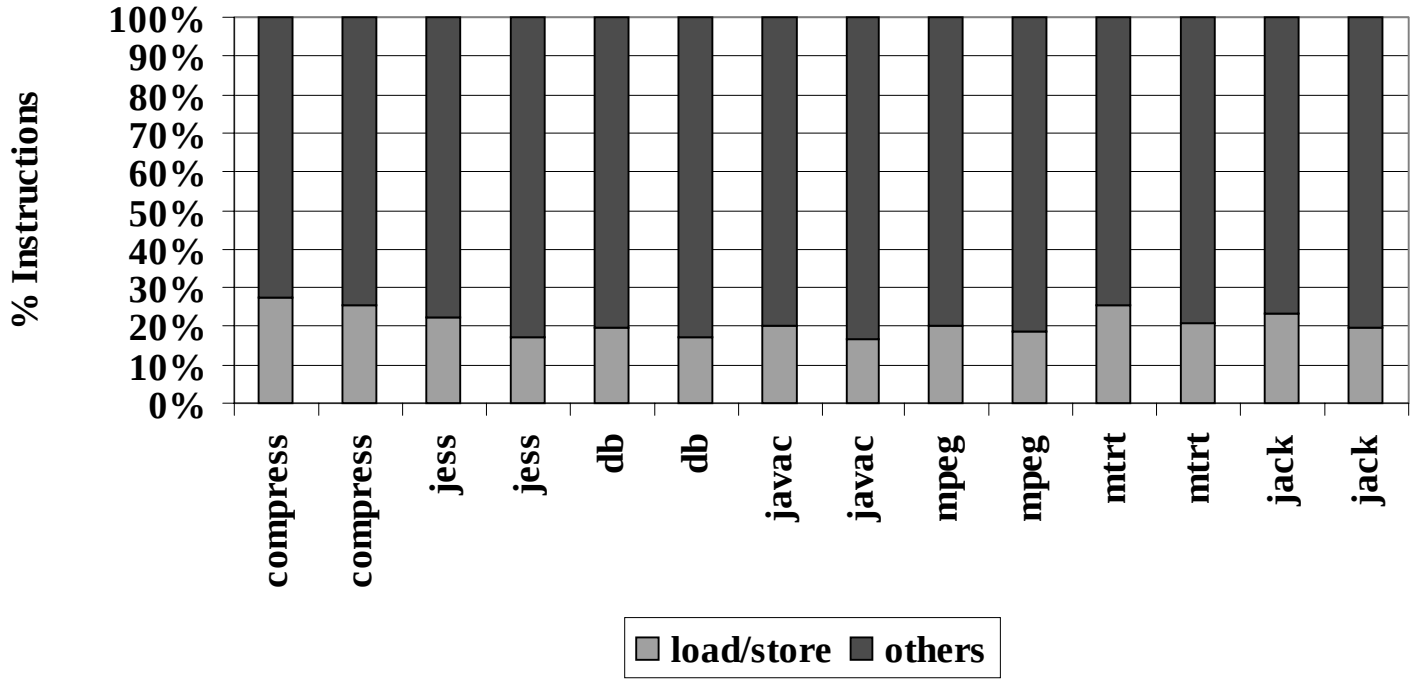
Energy Behavior of Java Codes

- SpecJVM benchmark codes
- Energy analysis
  - Hardware perspective
    - Which hardware components (e.g., datapath, caches, off-chip memory) consume what percentage of energy
  - Software perspective
    - Which portion of JVM consumes what percentage of energy
- Objective: Energy-aware JVM design

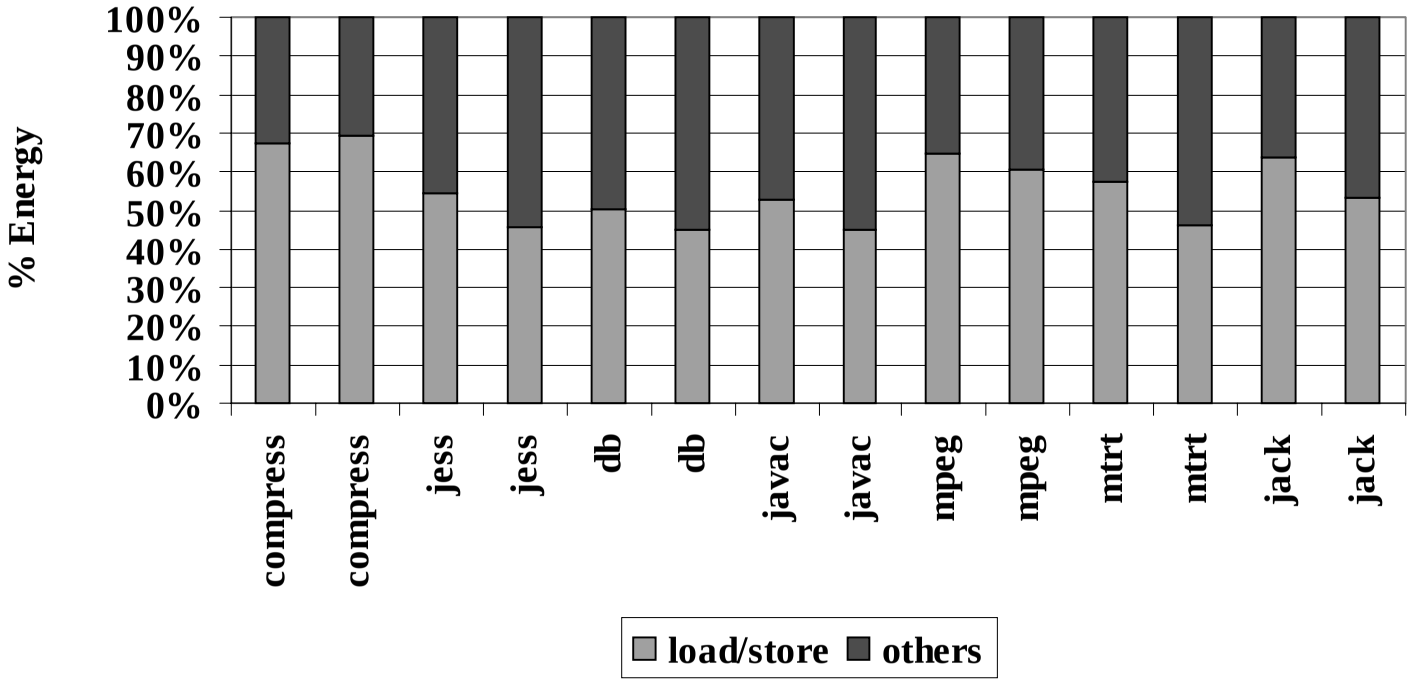
SpecJVM Benchmark Codes

Benchmark	Brief Description
compress	A high-performance application to compress/uncompress large files;based on the Lempel-Ziv method(LZW)
jess	A Java expert shell system based on NASA's CLIPS expert shell system
db	A small database management program that performs several database functions on a memory-resident database
javac	JDK 1.0.2 Java compiler
mpeg	MPEG-3 audio file compression application
mtrt	Dual-threaded ray tracer; the only multi-threaded application in the suite
jack	A Java parser generator with lexical analyzers; an early version of what is now called JavaCC

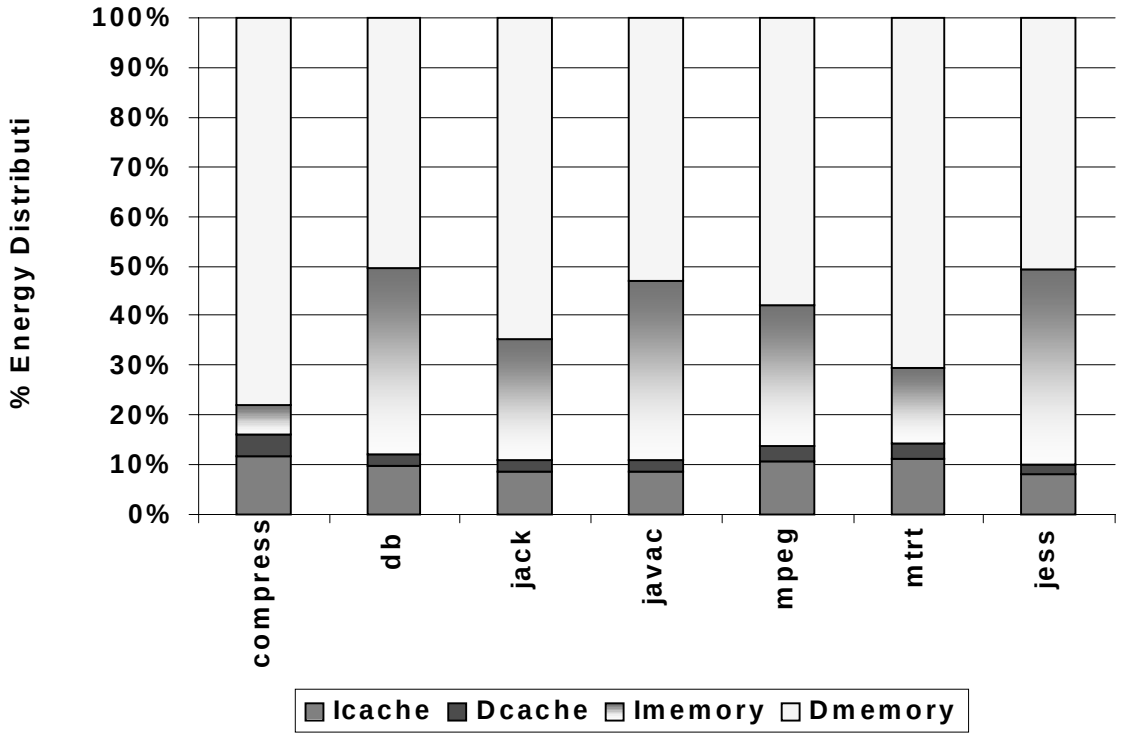
Percentage Distribution of Instructions



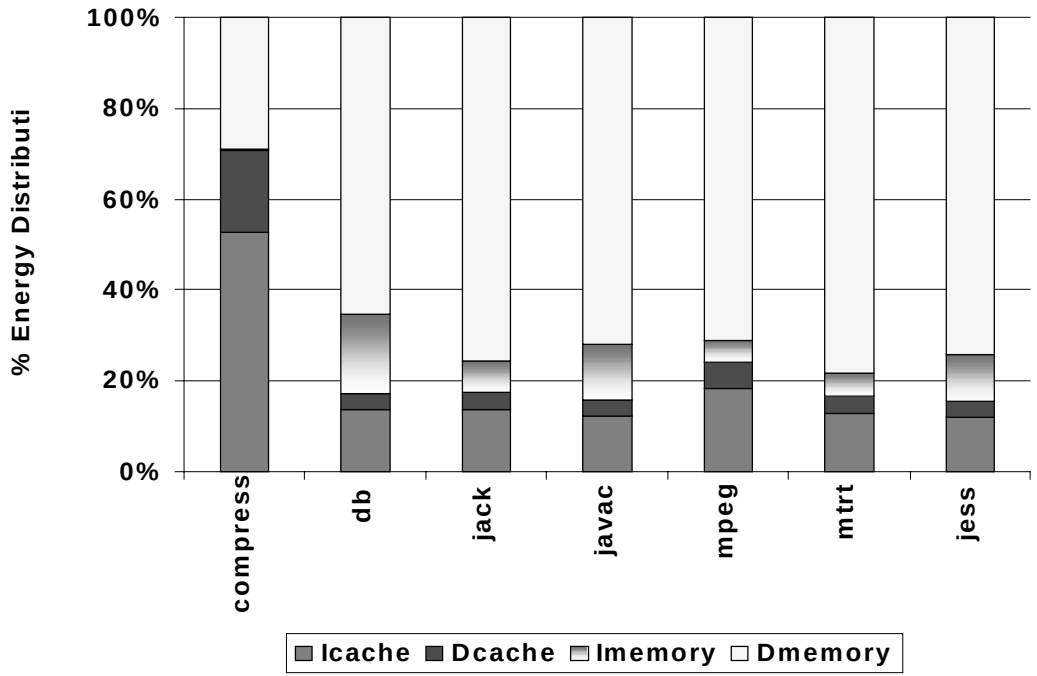
Energy Breakdown



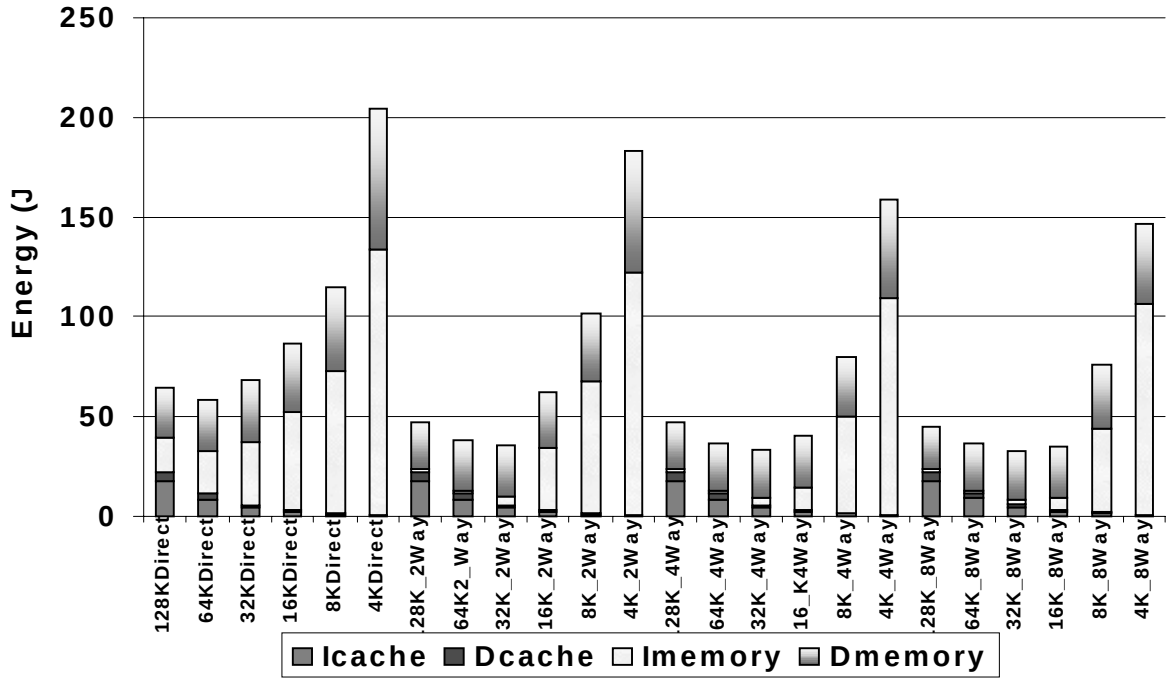
Energy Distribution for the JIT Mode (32KB 2-way set associative, 32 byte block size)



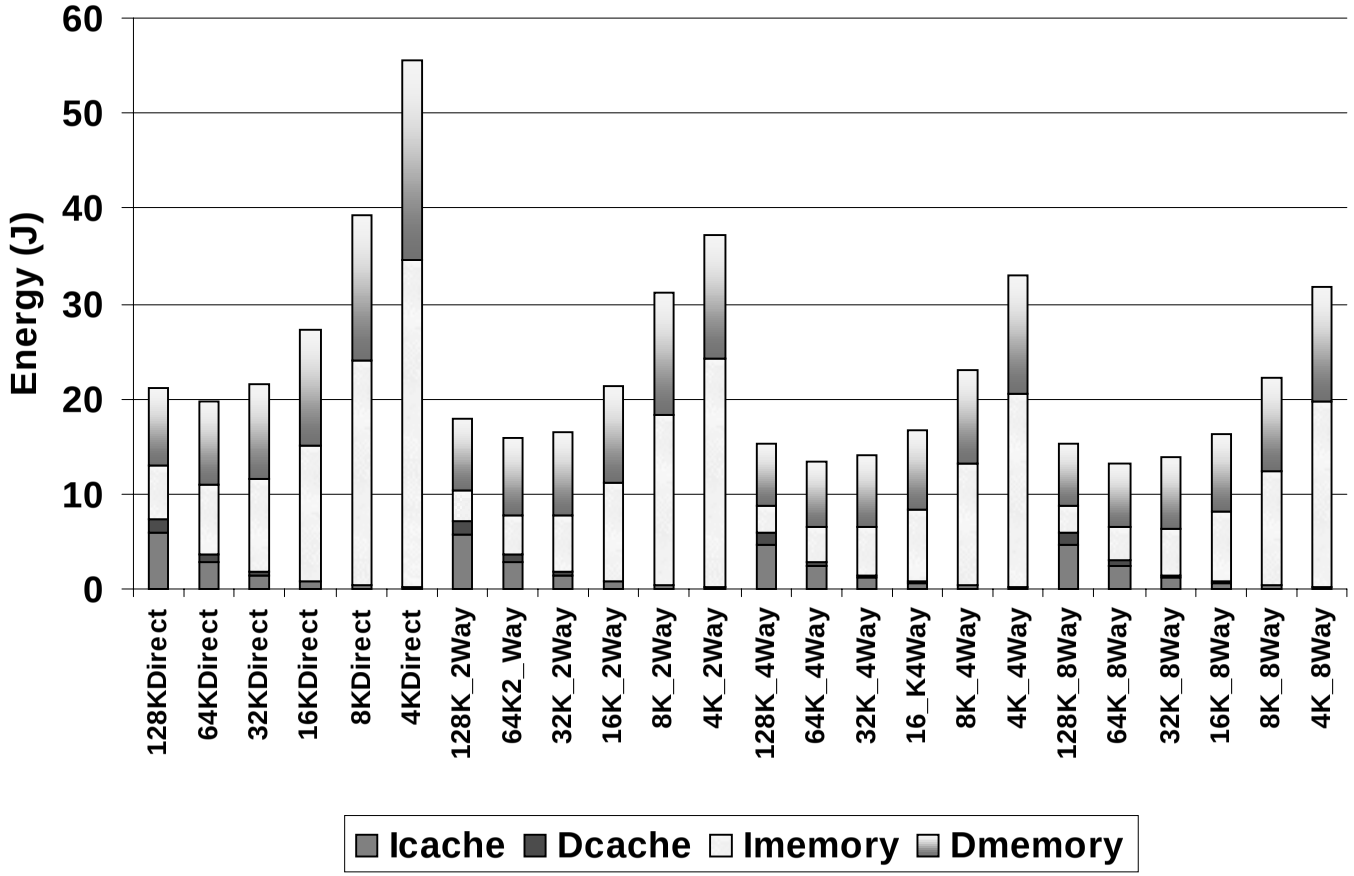
Energy Distribution for the Interpreter Mode (32KB 2-way set associative, 32 byte block)



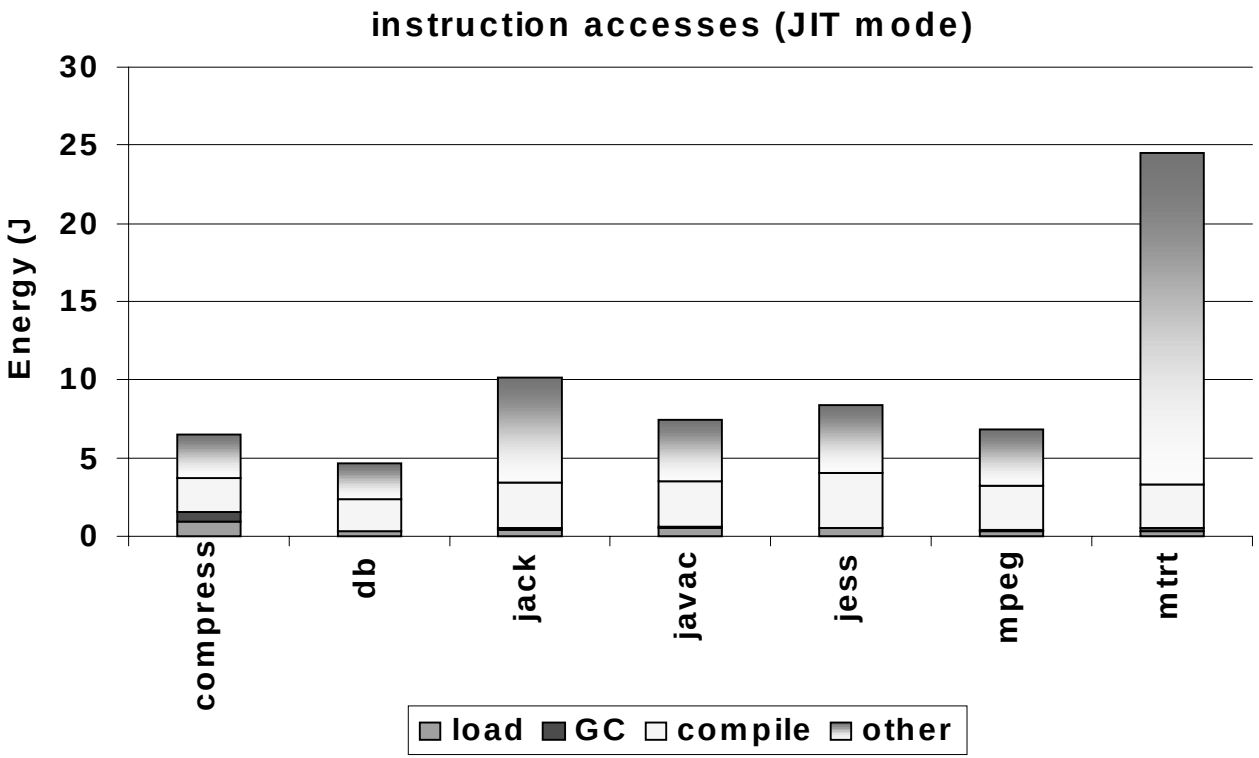
Energy Consumption of *javac* for the Interpreter Mode



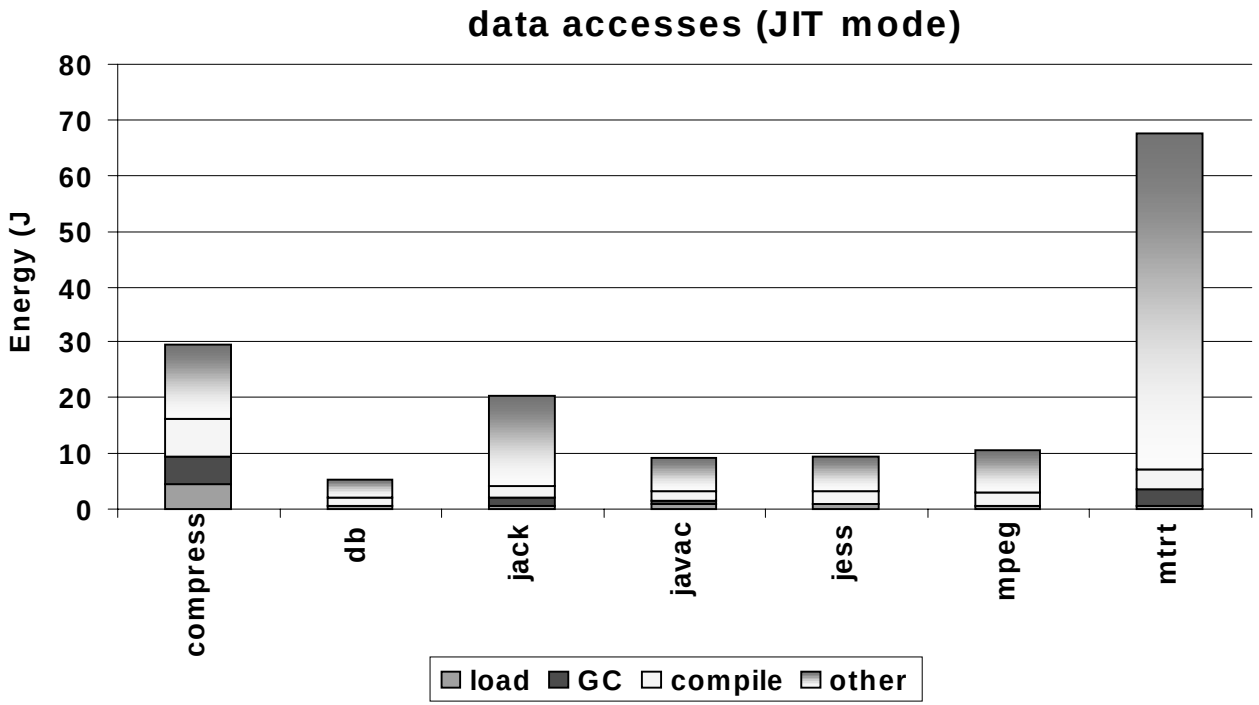
Energy Consumption of *javac* for the JIT Mode



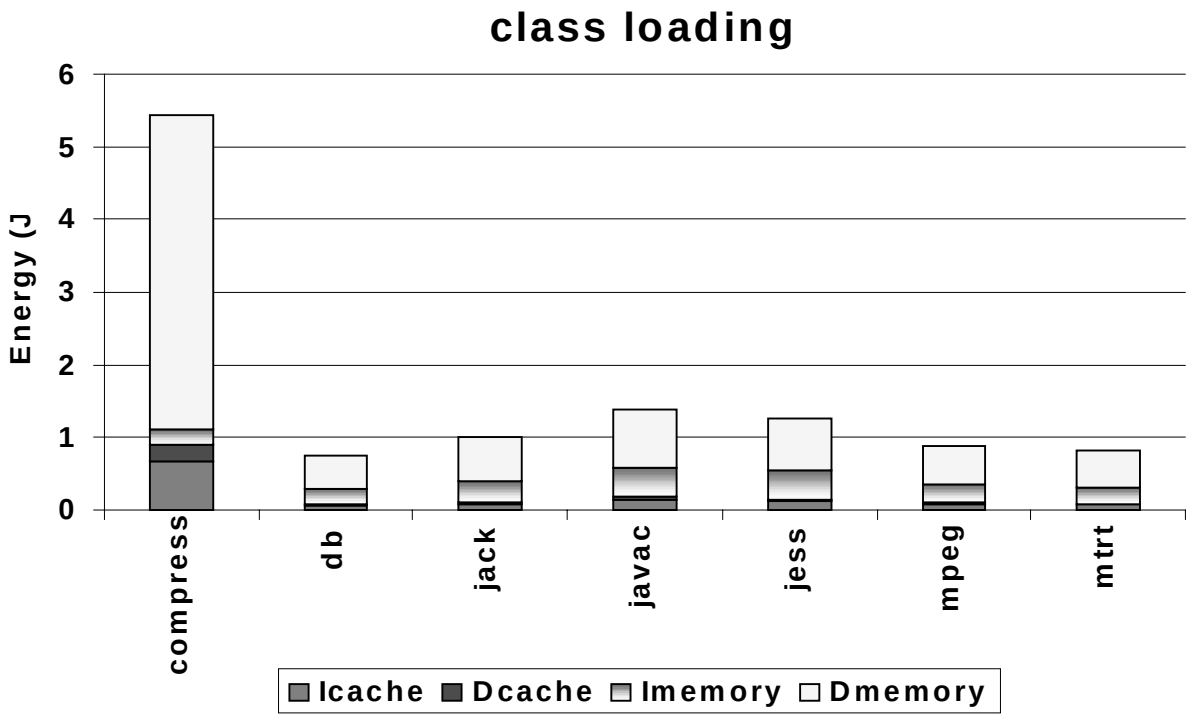
Energy Breakdown (Software View)



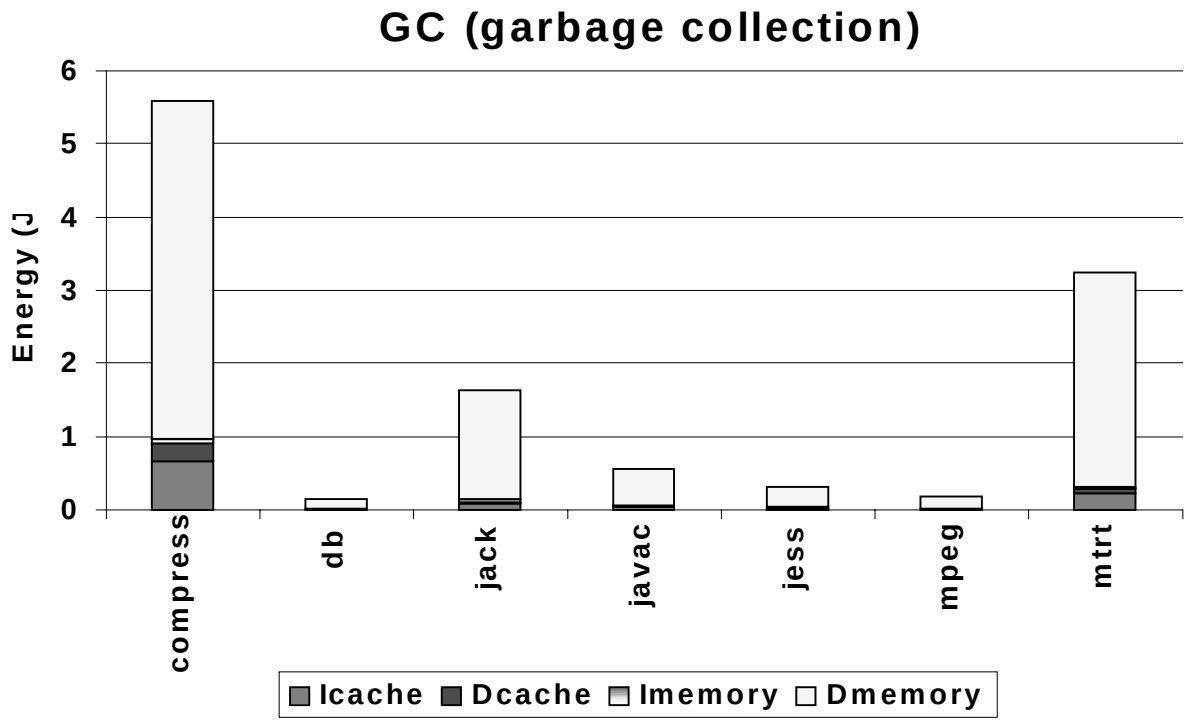
Energy Breakdown (Software View)



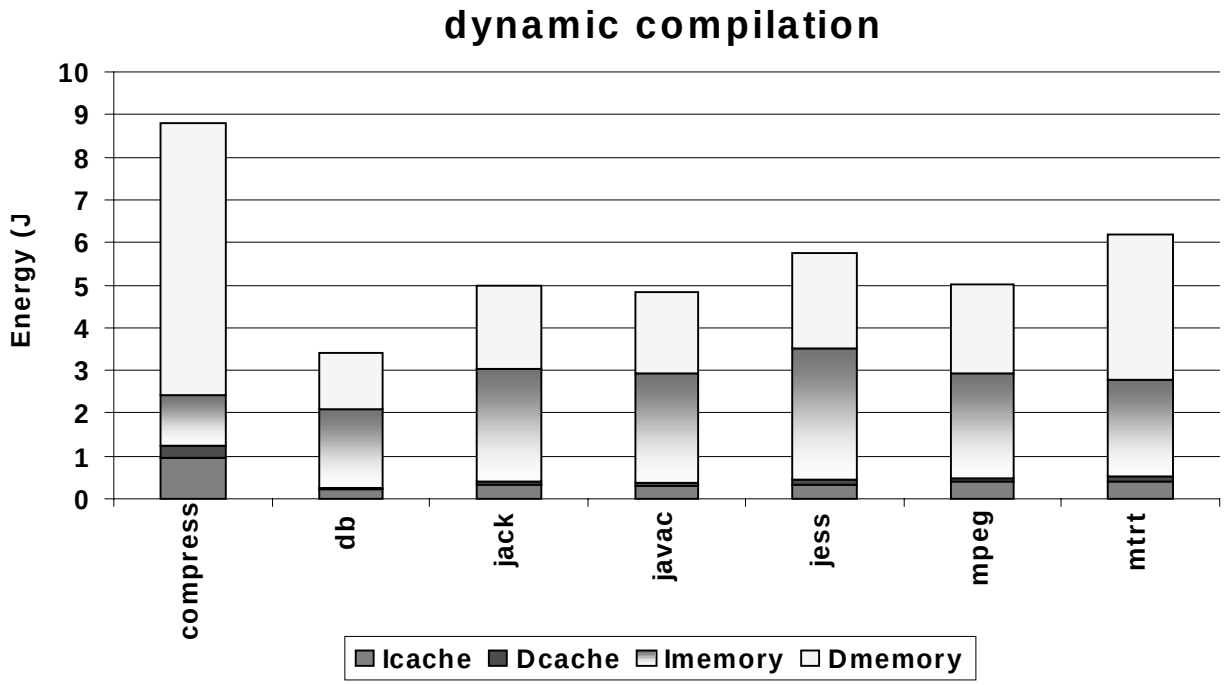
Energy Breakdown



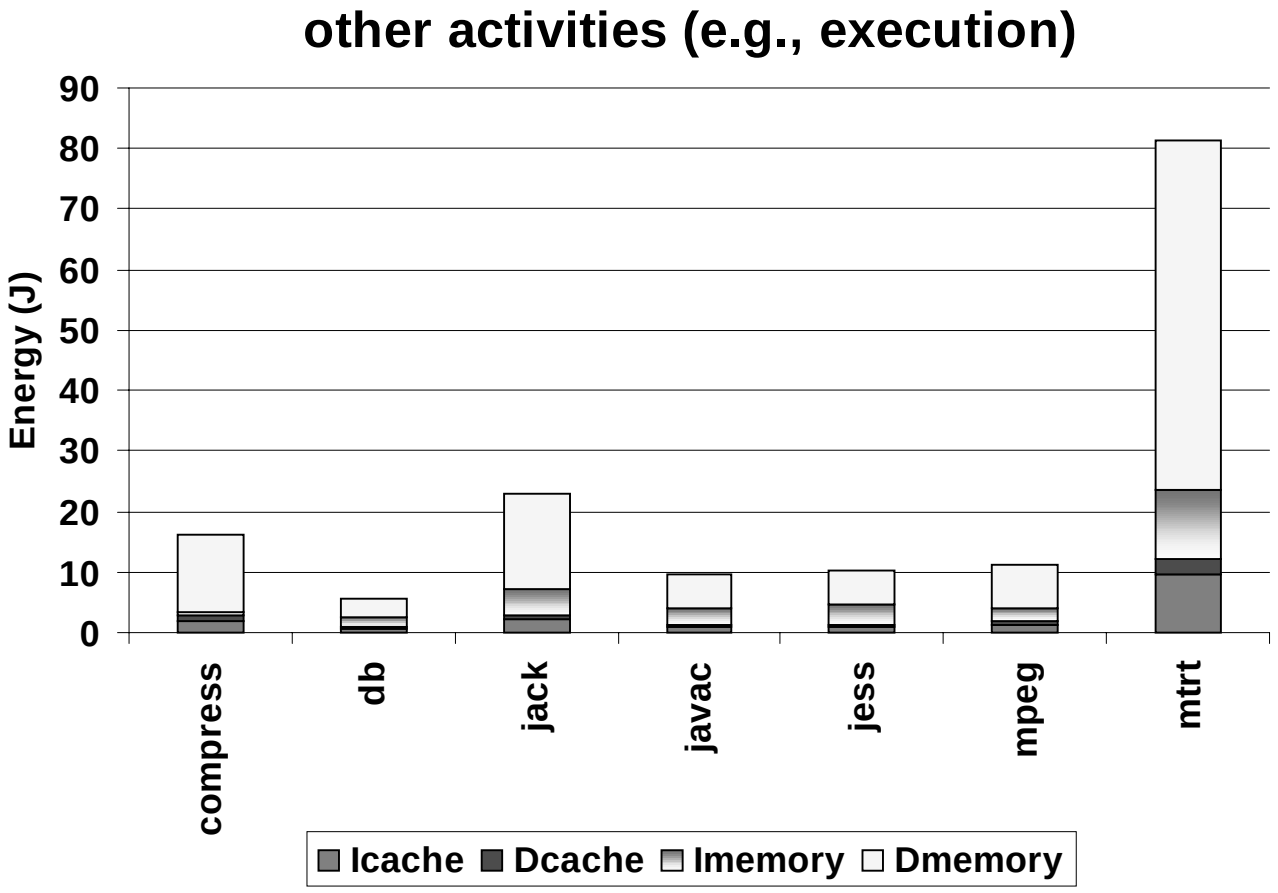
Energy Breakdown



Energy Breakdown



Energy Breakdown



lkkl

Conclusions

- SimplePower - cycle accurate simulator
  - Find energy hotspots in the architecture
  - Study hardware/software interaction
- Architectural experiments
  - Conventional architectures
  - Energy-efficient components
- Compiler optimization experiments
  - Classical optimizations (e.g., tiling, layout transformations)
  - Novel optimizations (e.g.,low-power mode control, partitioned memory)
  - JVM optimizations

Ongoing Work at Penn State

- Extending the energy simulator to
  - Superscalar machines (using SimpleScalar)
  - VLIW machines (using Trimaran)
- Clock energy and control circuitry modeling
- Energy-aware low-level optimizations
  - Instruction scheduling (basic block, beyond basic block)
  - Register re-labeling (post-compilation)
  - Register hierarchy management for low power
  - Code generation for an energy-conscious ISA
  - Energy-aware parallelization
- Energy-aware optimizing compiler and JVM

References

- Energy Simulator
  - The Design and Use of SimplePower: A Cycle-Accurate Energy Estimation Tool [DAC'00]
  - Energy Driven Integrated Hardware-Software Optimizations Using SimplePower [ISCA'00]
- Compiler Optimizations
  - Influence of Compiler Optimizations on System Power [DAC'00]
  - Memory System Energy: Hardware-Software Optimizations [ISLPED'00]
  - Experimental Evaluation of Energy Behavior of Tiling [LCPC'00]
  - Instruction Scheduling Based on Energy and Performance Constraints [VLSI Workshop'00]
  - Effect of Compiler Optimizations on Energy [SiPS'00]
  - Towards Energy-Aware Iteration Space Tiling [LCTES'00]
  - DRAM Energy Management Using Software and Hardware Directed Power Mode Control [HPCA'01]
- Hardware Optimizations
  - Multiple-Access Caches: Energy Implications [VLSI Workshop'00]
- JVM
  - Annotation Based Energy Optimization Using Array Interleaving [submitted to Workshop on Hardware Support for Objects and Microarchitectures for Java'00]

More Information

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