MINESH PATEL

Citizenship: USA ▪ *Address:* Houston, Texas, USA
https://www.mineshp.com ▪ minesh.patelh[at]gmail.com ▪ Google Scholar

RESEARCH INTERESTS

I am interested in the intersection between **computer architecture**, **systems**, and **dependability**, including:

- Architectures, programming interfaces, and runtime support for highly-efficient, cost-effective dependable systems capable of adapting to moving dependability goals (e.g., security, reliability, maintainability, etc.).
- Device and system design guidelines (e.g., standards, specifications) that facilitate transparency and informed decision-making during system design, analysis, modeling, and evaluation.
- System optimizations, mechanisms, and techniques to provide architectural, runtime and/or application control over how security and reliability concerns are addressed (e.g., prediction, detection, mitigation)

EDUCATION

2016-Apr 2022 — **ETH Zürich**, Zürich, Switzerland
Ph.D., Computer Engineering (adviser: Onur Mutlu)
Dissertation: **"***Enabling Effective Error Mitigation in Memory Chips That Use On-Die Error-Correcting Codes.***"** (DOI 10.3929/ethz-b-000542542)
2022 IEEE/IFIP William C. Carter Ph.D. Dissertation Award in Dependability.
2022 ETH Zürich Medal for Outstanding Doctoral Theses.

2015-2016 — **Carnegie Mellon University**, Pittsburgh, PA
Ph.D. in Electrical and Computer Engineering (transferred to ETH with adviser Onur Mutlu)

2011-2015 — **University of Texas at Austin**, Austin, TX (GPA: 3.97 / 4.00)
B.S. (Honors) Electrical and Computer Engineering
B.S. (Honors) Physics

PROFESSIONAL WORK EXPERIENCE

Mar–Aug 2019 — **Apple Inc:** Graduate Research Intern, SEG DRAM (Cupertino, CA, USA)

Jun–Sep 2018 — **Microsoft Research:** Research Intern, Mobility and Networking Group (Seattle, WA, USA)

May–Dec 2016, Jun–Dec 2017 — **Apple Inc:** Graduate Research Intern, Platform Architecture (Cupertino, CA, USA)
Explored memory subsystem performance and power opportunities using a combination of performance modeling and post-silicon main memory testing

May–Aug 2015 — **Microsoft:** Silicon Implementation Intern, HoloLens (Fort Collins, CO, USA)
Designed image processing hardware using high-level synthesis and Verilog

Jan–Aug 2014 — **Apple Inc:** Silicon Engineering Intern, SEG Graphics/GPU (Austin, TX, USA)
Functional model bring-up in C++ with multiple GPU driver APIs, including OpenGL

May–Aug 2013 — **National Instruments R&D:** HW Engineering (Digital Design) Intern (Austin, TX, USA)
Designed a CPLD-based CAT-II ch-ch isolated voltage module, verified prototype PCB

May–Aug 2012 — **General Electric:** ITLP Intern, UNIX/Linux Engineering Team (Cincinnati, OH, USA)
Evaluated Solaris-/SPARC-based virtualization technologies

HONORS AND AWARDS

Nov 2022	ETH Zürich Medal for Outstanding Doctoral Theses
Aug 2022	Intel Hardware Security Academic Award Finalist
June 2022	IEEE/IFIP William C. Carter Ph.D. Dissertation Award in Dependability
Sep 2021	International Symposium on Computer Architecture (ISCA) Hall of Fame
Oct 2020	Best Paper Award, MICRO (IEEE/ACM Int'l Symposium on Microarchitecture)
May 2020	IEEE Micro Top Picks Honorable Mention
Jun 2019	Best Paper Award, DSN (IEEE/IFIP Int'l Conference on Dependable Systems and Networks)
May 2015	Third Place Senior Design Project (UT EE464H – Mentor: Prof. Yale Patt)
May 2014	First Place in Autonomous Robot Racing (UT EE345M – Realtime Embedded Systems)
2011-2015	University of Texas Endowed Presidential Scholarship in ECE and Physics
2011-2015	University of Texas Engineering Honors Scholarship
2009	Eagle Scout Award

THESIS PUBLICATIONS

1. Minesh Patel, A. Giray Yaglikci, T. Shahroodi, A. Manglik, O. Mutlu. **"A Case for Transparent Reliability in DRAM Systems."**
   arXiv:2204.10378, Apr. 2022.
   Open-source dataset: https://github.com/CMU-SAFARI/DRAM-Datasheet-Survey

2. Minesh Patel, G. F. de Oliveira Jr., O. Mutlu. **"HARP: Practically and Effectively Identifying Uncorrectable Errors in Main Memory Chips That Use On-Die ECC."**
   To appear in *International Symposium on Microarchitecture (MICRO-54)*, Oct. 2021.
   Officially Artifact Evaluated as Available, Reusable and Reproducible.
   Open-source artifacts: https://github.com/CMU-SAFARI/HARP

3. Minesh Patel, J. S. Kim, T. Shahroodi, H. Hassan, and O. Mutlu. "**Bit-Exact ECC Recovery (BEER): Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics**."
   International Symposium on Microarchitecture (MICRO-53), Oct. 2020.
   Best Paper Award.
   Open-source code: https://github.com/CMU-SAFARI/BEER

4. Minesh Patel, J. S. Kim, H. Hassan, and O. Mutlu. **"Understanding and Modeling On-Die Error Correction in Modern DRAM: An Experimental Study Using Real Devices."**
   IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-49), Jun. 2019.
   Best Paper Award.
   Open-source code: https://github.com/CMU-SAFARI/EINSim

5. Minesh Patel, J. S. Kim, and O. Mutlu. **"The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions."**
   International Symposium on Computer Architecture (ISCA-44), Jun. 2017.

PEER-REVIEWED PUBLICATIONS

1. G. Yaglikci, H. Luo, G. F. de Oliviera Jr., A. Olgun, Minesh Patel, J. Park, H. Hassan, J. S. Kim, L. Orosa, and O. Mutlu, **"Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices"**
   IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-52), Jun. 2022.

2. Minesh Patel, G. F. de Oliveira Jr., O. Mutlu. **"HARP: Practically and Effectively Identifying Uncorrectable Errors in Main Memory Chips That Use On-Die ECC."**
   International Symposium on Microarchitecture (MICRO-54), Oct. 2021.
   Officially Artifact Evaluated as Available, Reusable and Reproducible.
   Open-source artifacts: https://github.com/CMU-SAFARI/HARP

3. L. Orosa, G. Yaglikci, H. Luo, A. Olgun, J. Park, H. Hassan, Minesh Patel, J. S. Kim, O. Mutlu. **"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses"**
   International Symposium on Microarchitecture (MICRO-54), Oct. 2021.

4. Ataberk Olgun, Minesh Patel l, A. Giray Yaglikci, Haocong Luo, Jeremie S. Kim, F. Nisa Bostanci, Nandita Vijaykumar, Oguz Ergin, and Onur Mutlu. **"QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips."**
   International Symposium on Computer Architecture (ISCA-48), Jun. 2021.

5. Lois Orosa, Yaohua Wang, Mohammad Sadrosadati, Jeremie S. Kim, Minesh Patel, Ivan Puddu, Haocong Luo, Kaveh Razavi, Juan Gomez-Luna, Hasan Hassan, Nika Mansouri-Ghiasi, Saugata Ghose, and Onur Mutlu. **"CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations."**
   International Symposium on Computer Architecture (ISCA-48), Jun. 2021.

6. Nastaran Hajinazar, Geraldo F. Oliveira, Sven Gregorio, Joao Dinis Ferreira, Nika Mansouri Ghiasi, Minesh Patel, Mohammed Alser, Saugata Ghose, Juan Gomez-Luna, and Onur Mutlu. "**SIMDRAM: An End-to-End Framework for Bit-Serial SIMD Computing in DRAM.**"
   International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-26), Mar.-Apr. 2021.

7. A. G. Yaglikci, Minesh Patel, J. S. Kim, R. Azizi, A. Olgun, L. Orosa, H. Hassan, J. Park, K. Kanellopoulos, T. Shahroodi, S. Ghose, and O. Mutlu. "**BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows.**"
   International Symposium on High-Performance Computer Architecture (HPCA-27), Feb. 2021.
   Intel Hardware Security Academic Award Finalist 2022.

8. Minesh Patel, J. S. Kim, T. Shahroodi, H. Hassan, and O. Mutlu. "**Bit-Exact ECC Recovery (BEER): Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics**."
   International Symposium on Microarchitecture (MICRO-53), Oct. 2020.
   Best Paper Award.
   Open-source code: https://github.com/CMU-SAFARI/BEER

9. Y. Wang, L. Orosa, X. Peng, Y. Guo, S. Ghose, Minesh Patel, J. S. Kim, J. G. Luna, M. Sadrosadati, N. M. Ghiasi, and O. Mutlu. **"FIGARO: Improving System Performance via Fine-Grained In-DRAM Data Relocation and Caching."**
International Symposium on Microarchitecture (MICRO-53), Oct. 2020.

10. J. S. Kim, Minesh Patel, A. G. Yaglikci, H. Hassan, R. Azizi, L. Orosa, and O. Mutlu. **"Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques."**
International Symposium on Computer Architecture (ISCA-47), Jun. 2020.

11. H. Luo, T. Shahroodi, H. Hassan, Minesh Patel, A. G. Yaglikci, L. Orosa, J. Park, and O. Mutlu. **"CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-Off."**
International Symposium on Computer Architecture (ISCA-47), Jun. 2020.

12. N. Hajinazar, P. Patel, Minesh Patel, K. Kanellopoulos, S. Ghose, R. Ausavarungnirun, G. F. de Oliveira Jr., J. Appavoo, V. Seshadri, and O. Mutlu. **"The Virtual Block Interface: A Flexible Alternative to the Conventional Virtual Memory Framework."**
International Symposium on Computer Architecture (ISCA-47), Jun. 2020.

13. L. Cojocar, J. S. Kim, Minesh Patel, L. Tsai, S. Saroiu, A. Wolman, and O. Mutlu. **"Are We Susceptible to Rowhammer? An End-to-End Methodology for Cloud Providers."**
IEEE Symposium on Security and Privacy (S&P-41), May 2020.

14. H. Hassan, Minesh Patel, J. S. Kim, A. G. Yaglikci, N. Vijaykumar, N. M. Ghiasi, S. Ghose, and O. Mutlu. **"CROW: A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability."**
International Symposium on Computer Architecture (ISCA-46), Jun. 2019.

15. A. Boroumand, S. Ghose, Minesh Patel, H. Hassan, B. Lucia, R. Ausavarungnirun, K. Hsieh, N. Hajinazar, K. T. Malladi, H. Zheng, and O. Mutlu. **"CoNDA: Efficient Cache Coherence Support for Near-Data Accelerators."**
International Symposium on Computer Architecture (ISCA-46), Jun. 2019.

16. Minesh Patel, J. S. Kim, H. Hassan, and O. Mutlu. **"Understanding and Modeling On-Die Error Correction in Modern DRAM: An Experimental Study Using Real Devices."**
IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-49), Jun. 2019.
Best Paper Award.
Open-source code: https://github.com/CMU-SAFARI/EINSim

17. J. S. Kim, Minesh Patel, H. Hassan, L. Orosa, and O. Mutlu. **"D-RaNGe: Using Commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput."**
International Symposium on High-Performance Computer Architecture (HPCA-25), Feb. 2019.
IEEE Micro Top Picks Honorable Mention.

18. Y. Wang, A. Tavakkol, L. Orosa, S. Ghose, N. M. Ghiasi, Minesh Patel, J. S. Kim, H. Hassan, M. Sadrosadati, and O. Mutlu. **"Reducing DRAM Latency via Charge-Level-Aware Look-Ahead Partial Restoration."**
International Symposium on Microarchitecture (MICRO-51), Oct. 2018.

19. J. S. Kim, Minesh Patel, H. Hassan, and O. Mutlu. **"Solar-DRAM: Reducing DRAM Access Latency by Exploiting the Variation in Local Bitlines**."
IEEE International Conference on Computer Design (ICCD-36), Oct. 2018.

20. J. S. Kim, Minesh Patel, H. Hassan, and O. Mutlu. **"The DRAM Latency PUF: Quickly Evaluating Physical Unclonable Functions by Exploiting the Latency-Reliability Tradeoff in Modern DRAM Devices."**
International Symposium on High-Performance Computer Architecture (HPCA-24), Feb. 2018.

21. Minesh Patel, J. S. Kim, and O. Mutlu. **"The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions."**
International Symposium on Computer Architecture (ISCA-44), Jun. 2017.

22. A. Boroumand, S. Ghose, Minesh Patel, H. Hassan, B. Lucia, K. Hsieh, K. T. Malladi, H. Zheng, and O. Mutlu. **"LazyPIM: An Efficient Cache Coherence Mechanism for Processing-in-Memory."**
IEEE Computer Architecture Letters (CAL), Jun. 2016.

DOCTORAL DISSERTATION

1. Minesh Patel, **"Enabling Effective Error Mitigation In Memory Chips That Use On-Die Error-Correcting Codes."**
Ph.D. Dissertation, ETH Zürich, Apr 2022.
DOI 10.3929/ethz-b-000542542
2022 IEEE/IFIP William C. Carter Ph.D. Dissertation Award in Dependability.
2022 ETH Zürich Medal for Outstanding Doctoral Theses.

PATENTS

J. S. Kim, Minesh Patel, S. Meier, T. Huberty, O. Mutlu. **"Security Techniques Based on Memory Timing Characteristics."** *U.S. Patent US10776521B2*. Sep. 2020.

TEACHING EXPERIENCE

2017-2021	**Computer Architecture** (MS Level), ETH Zurich, *Teaching Assistant*
2020-2021	**Digital Design and Computer Architecture** (BS Level), ETH Zurich, *Teaching Assistant*
2017-2019	**Digital Design and Circuits** (BS Level), ETH Zurich, *Teaching Assistant*
2017-2021	**Seminar in Computer Architecture** (BS Level), ETH Zurich, *Teaching Assistant*
2011-2013	**PHY303K, PS303, PHY355** (UT Mechanics, Intro to Modern Physics), *Teaching Assistant*
2011-2013	**Sanger Learning Center** (Introductory Physics and Mathematics), *Tutor*

STUDENT MENTORSHIP

- **ETH Zürich Ph.D. and Master's Students**
A. Giray Yaglikci (2019-2022), Haocong Luo (2019-2021), Ataberk Olgun (2020-2021), Aditya Manglik (2020-2022), Taha Shahroodi (2019-2021), Roknoddin Azizi (2019-2021)

- **ETH Zürich Undergraduate Students**
Jonas Elmiger (2021), Hong Chul Nam (2021)

OPEN-SOURCE TOOLS/INFRASTRUCTURE

DRAM Datasheet Survey: Historical survey of DRAM chip parameters and operating timings in chip datasheets
https://github.com/CMU-SAFARI/DRAM-Datasheet-Survey

HARP: C++/SMT tool for studying main memory error injection and profiling
https://github.com/CMU-SAFARI/HARP

BEER: C++/Python/SMT tool for analyzing and reverse-engineering DRAM error-correcting codes (ECCs)
https://github.com/CMU-SAFARI/BEER

EINSim: C++ Monte-Carlo simulator for exploring how error-correcting codes (ECCs) impact DRAM errors
https://github.com/CMU-SAFARI/EINSim

CONFERENCE TALKS

1. **HARP: Practically and Effectively Identifying Uncorrectable Errors in Main Memory Chips That Use On-Die ECC."** *International Symposium on Microarchitecture (MICRO-54)*, Virtual, Oct. 2021.

2. **"Bit-Exact ECC Recovery (BEER): Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics**," *International Symposium on Microarchitecture (MICRO-53)*, Virtual, Oct. 2020.

3. **"Understanding and Modeling On-Die Error Correction in Modern DRAM: An Experimental Study Using Real Devices"**, *International Conference on Dependable Systems and Networks (DSN-49)*, Portland, OR, Jun. 2019

4. **"The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions"**, *International Symposium on Computer Architecture (ISCA-44)*, Toronto, Canada, Jun. 2017.

INVITED TALKS

1. **"Enabling Effective Error Mitigation in Systems that Use Memory Chips with On-Die Error Correction"**
   Stanford University, Palo Alto, California, Nov 2022

2. **Award Acceptance Speech: William C. Carter PhD Dissertation Award in Dependability**
   IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-52), Baltimore, MD, Jun. 2022.
   [video recording] [slides (pdf/pptx)]

3. **"HARP: Practically and Effectively Identifying Uncorrectable Errors in Memory Chips That Use On-Die Error-Correcting Codes**"
   Invited Lecture, *"Computer Architecture"*, ETH Zürich, Nov. 2021.
   International Symposium on Microarchitecture (MICRO-54), Virtual, Oct. 2021.
   [video recording] [slides (pdf/pptx)]

4. **"Enabling Effective Error Mitigation in Memory Chips That Use On-Die Error-Correcting Codes"**
   SAFARI Live Seminar, Virtual, Sep. 2021.
   [video recording]

5. **"Bit-Exact ECC Recovery (BEER): Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics**"
   Invited Lecture, *"Computer Architecture"*, ETH Zürich, Oct. 2020.
   International Symposium on Microarchitecture (MICRO-53), Virtual, Oct. 2020.
   [video recording] [slides (pdf/pptx)]

6. **"Understanding and Modeling On-Die Error Correction in Modern DRAM: An Experimental Study Using Real Devices"**
   Invited Lecture, *"Computer Architecture",* ETH Zürich, Oct. 2019.
   International Conference on Dependable Systems and Networks (DSN-49), Portland, OR, Jun. 2019.
   [video recording] [slides (pdf/pptx)]

7. **"Timing and Verification"**
   Invited Lecture, *"Design of Digital Circuits",* ETH Zürich, Mar. 2018.
   [video recording] [slides (pdf/pptx)]

8. **"The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions"**
   Invited Lecture, *"Seminar on Computer Architecture",* ETH Zürich, Sep. 2019.
   Invited Lecture, *"Computer Architecture",* ETH Zürich, Oct. 2018.
   "ETH Zürich Systems Group Industry Retreat", Engelberg, Switzerland, Jan. 2018.
   International Symposium on Computer Architecture (ISCA-44), Toronto, Canada, Jun. 2017.
   [slides (pdf/pptx)]

SERVICE

- *Technical Program Committee Member*: Int'l. Conf. on Dependable Systems and Networks (DSN) 2023
- *Technical Reviewer for Conferences:* ISCA, MICRO, HPCA, ASPLOS, DSN, Usenix Security Symposium, Usenix ATC, DAC, PLDI, ICS, ISPASS, FAST, PACT, HotStorage
- *Technical Reviewer for Journals:* IEEE Transactions on Computers (TOC), IEEE Computer Architecture Letters (CAL), Microelectronics Reliability, IEEE Transactions on Circuits and Systems (TCAS), IEEE Transactions on Computer Aided Design (TCAD), IEEE Transactions on Electron Devices (TED), ACM Transactions on Embedded Computing Systems (TECS), IEEE Micro Top Picks, ACM Journal on Emerging Technologies in Computing Systems, ACM Transactions on Architecture and Code Optimization (TACO)
- *IT Infrastructure Co-Lead*, SAFARI Research Group, ETH Zürich 2019-2021
- *Lab Event Coordinator*, SAFARI Research Group, ETH Zürich 2019-2021