CROW

A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability

Hasan Hassan

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ETH zürich

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Summary

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Challenges of DRAM scaling:

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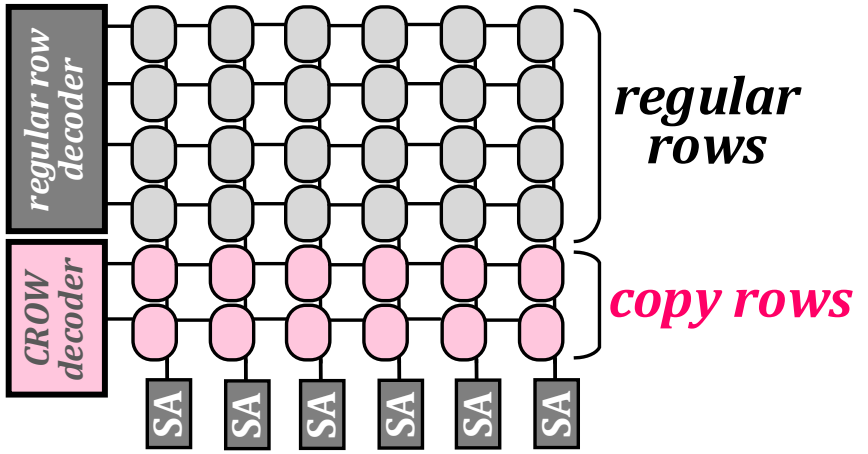

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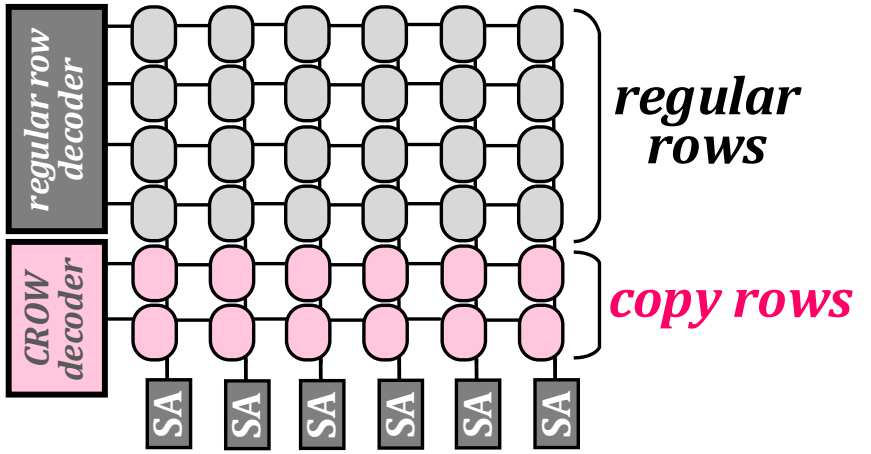

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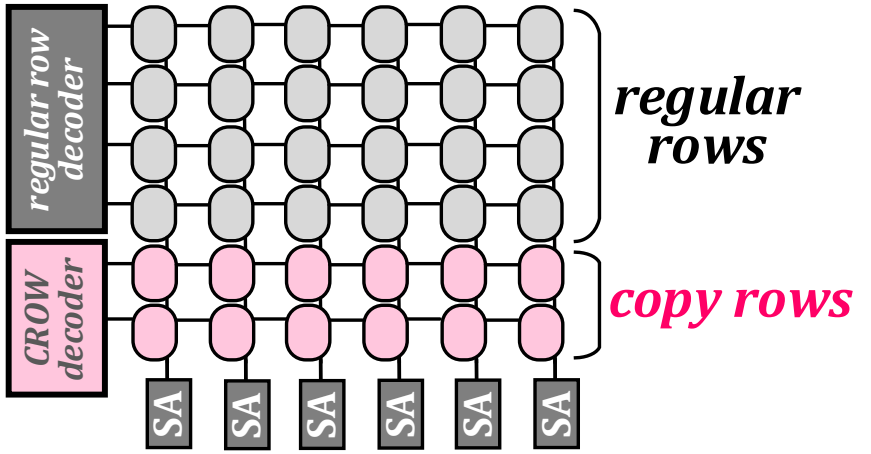

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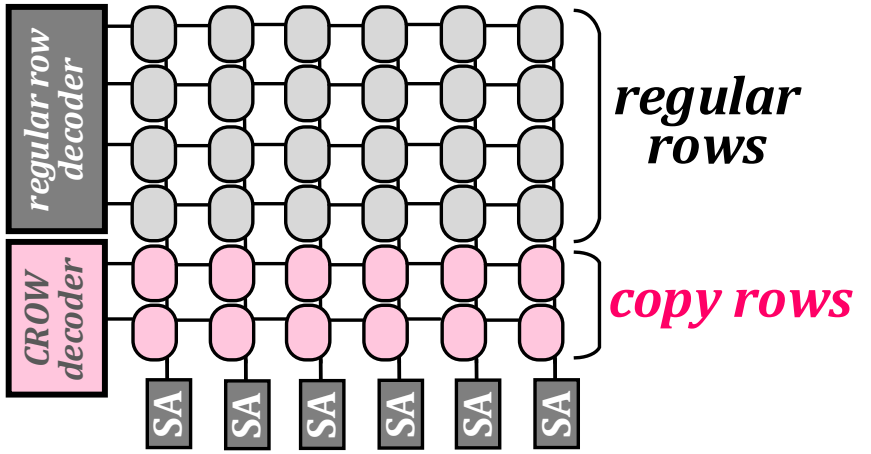

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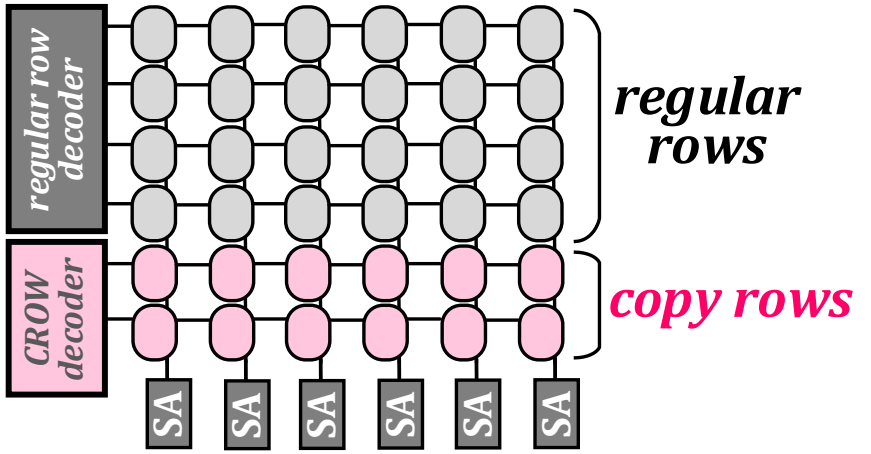

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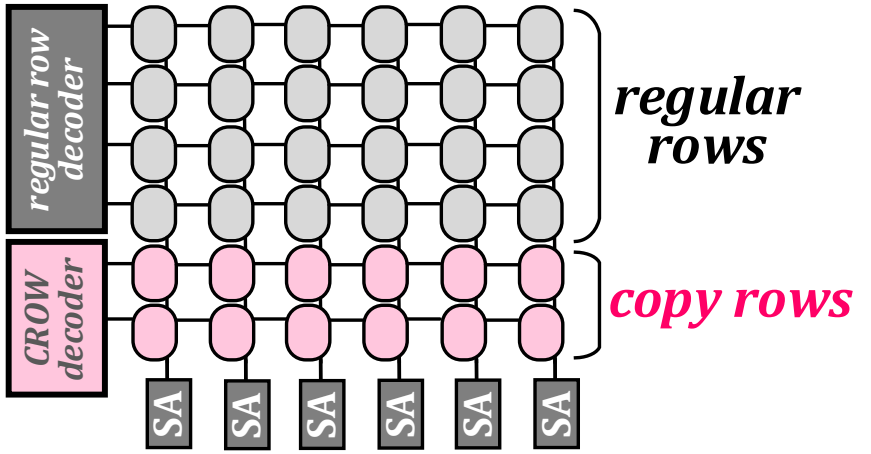

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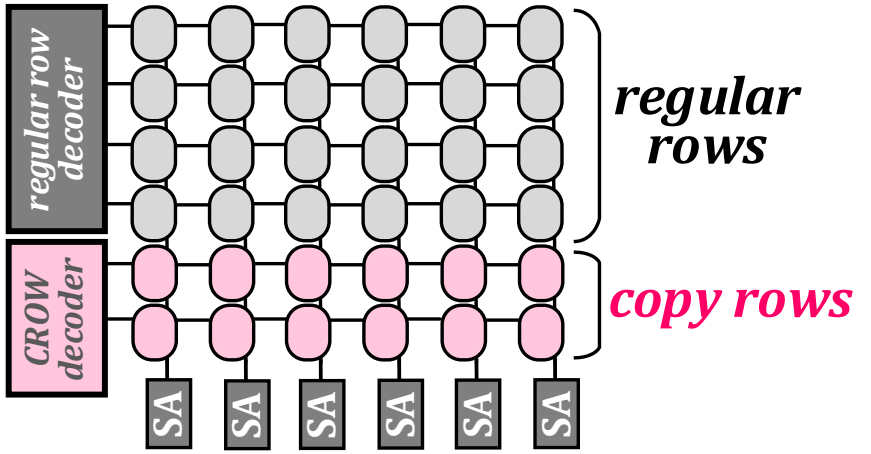

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Source code available in July:
github.com/CMU-SAFARI/CROW

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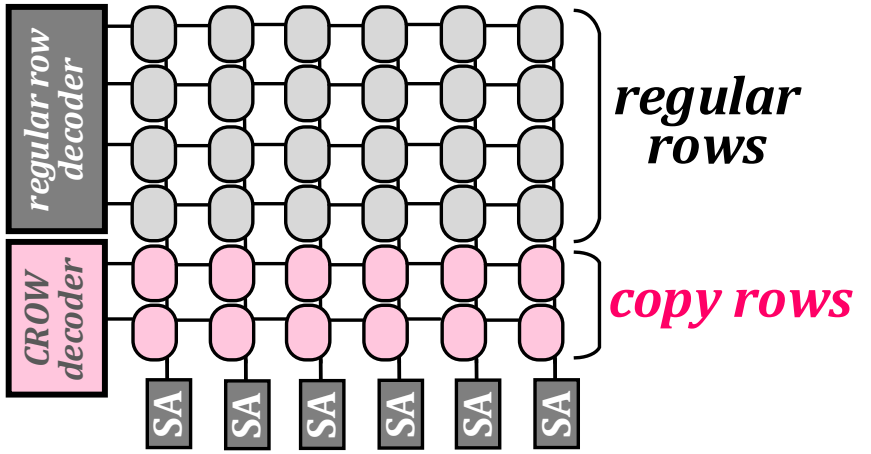

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Memory Controller

CPU

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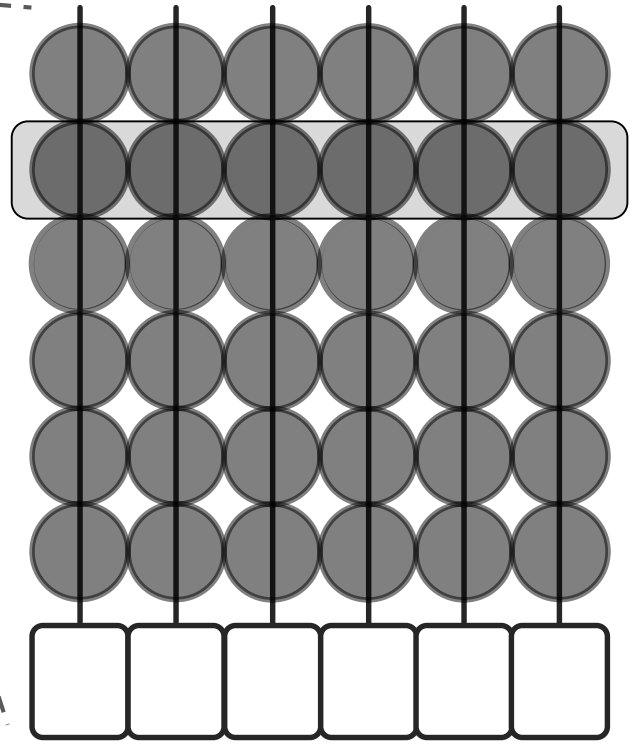
DRAM Subarray



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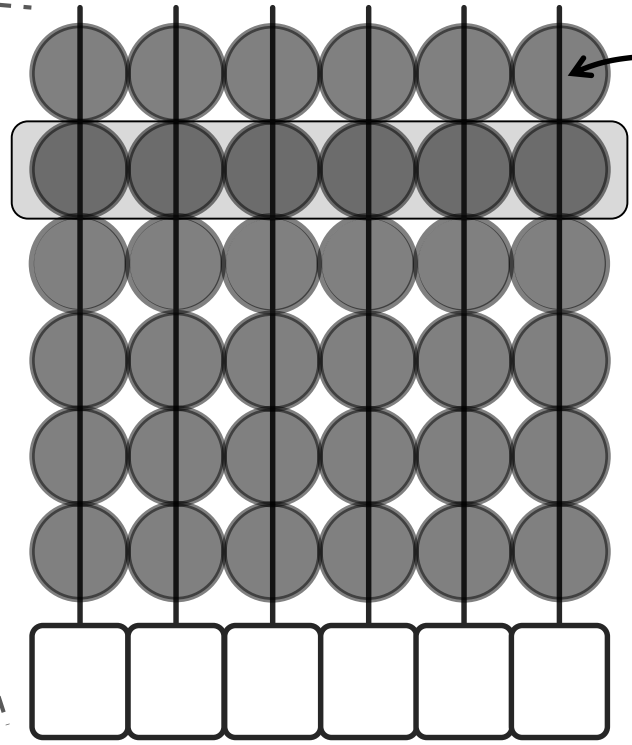

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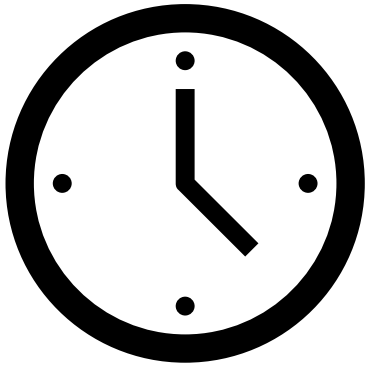
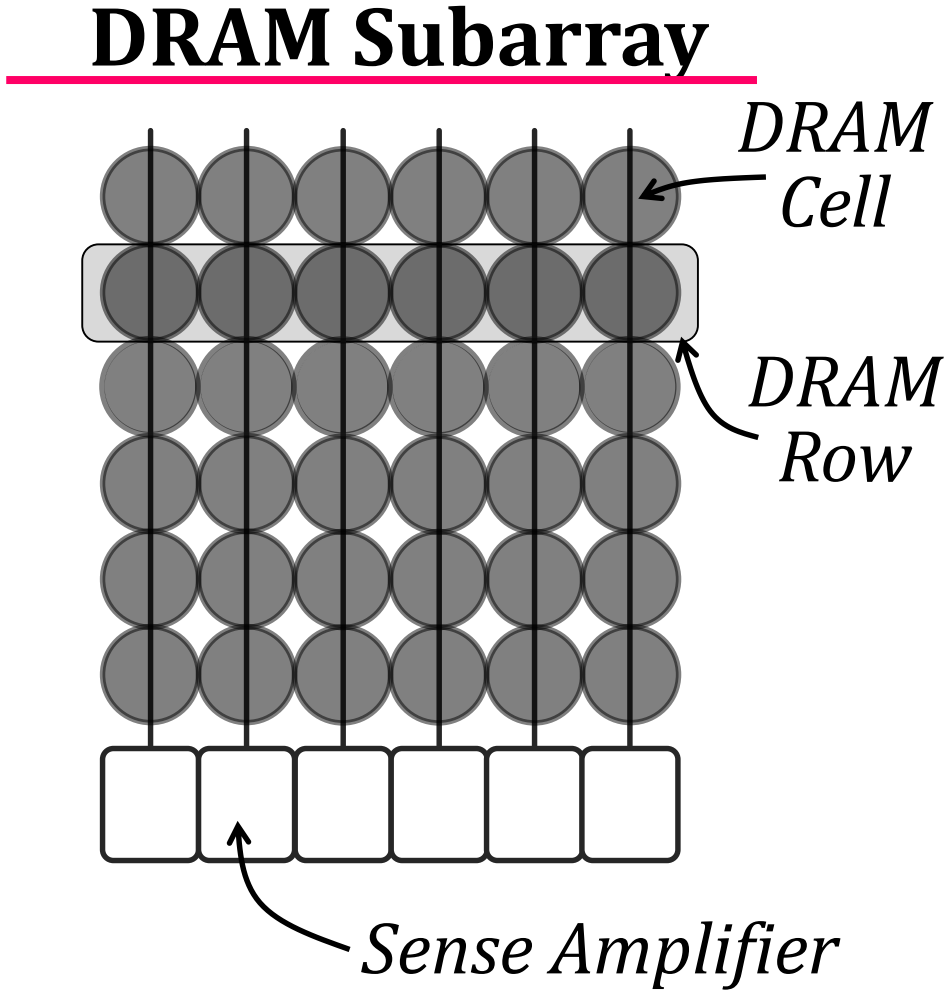
Accessing DRAM





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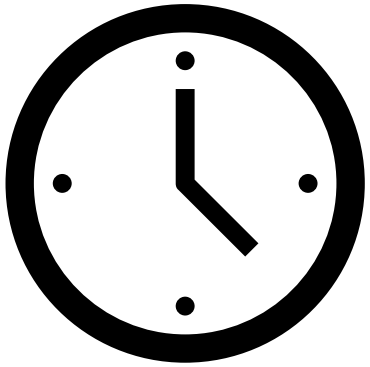

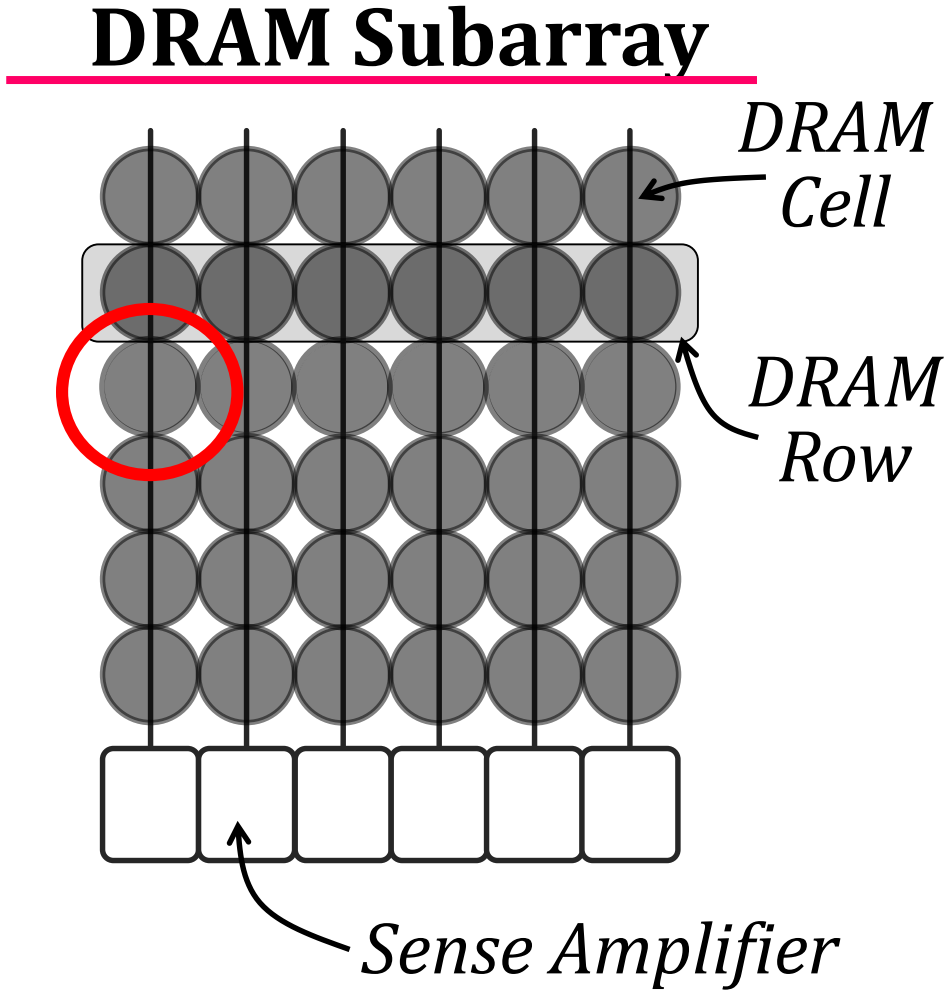

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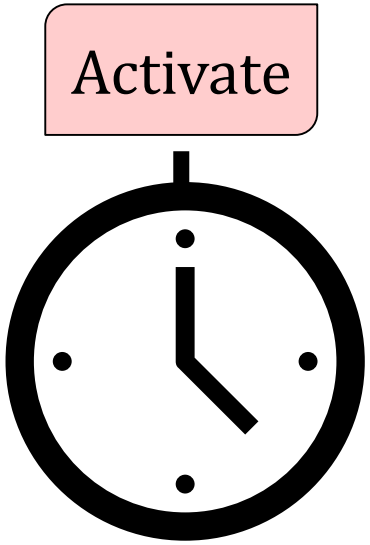

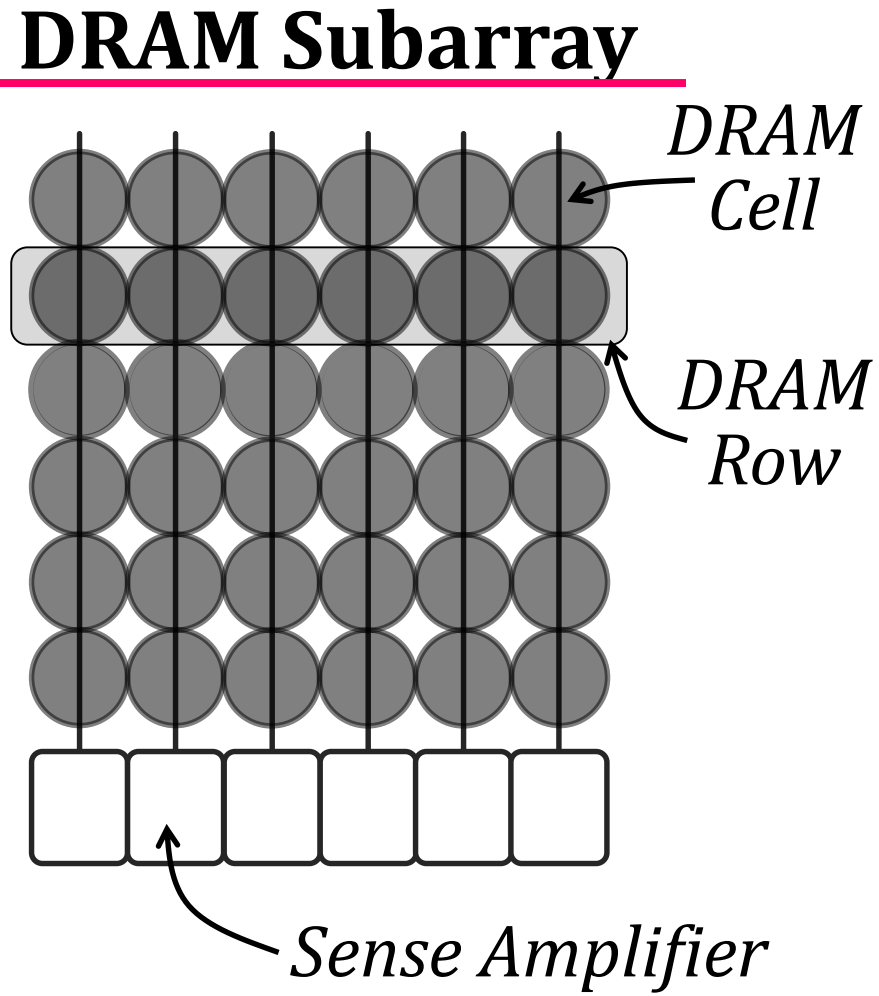

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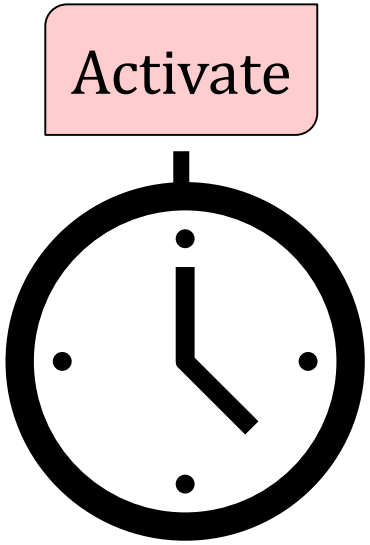

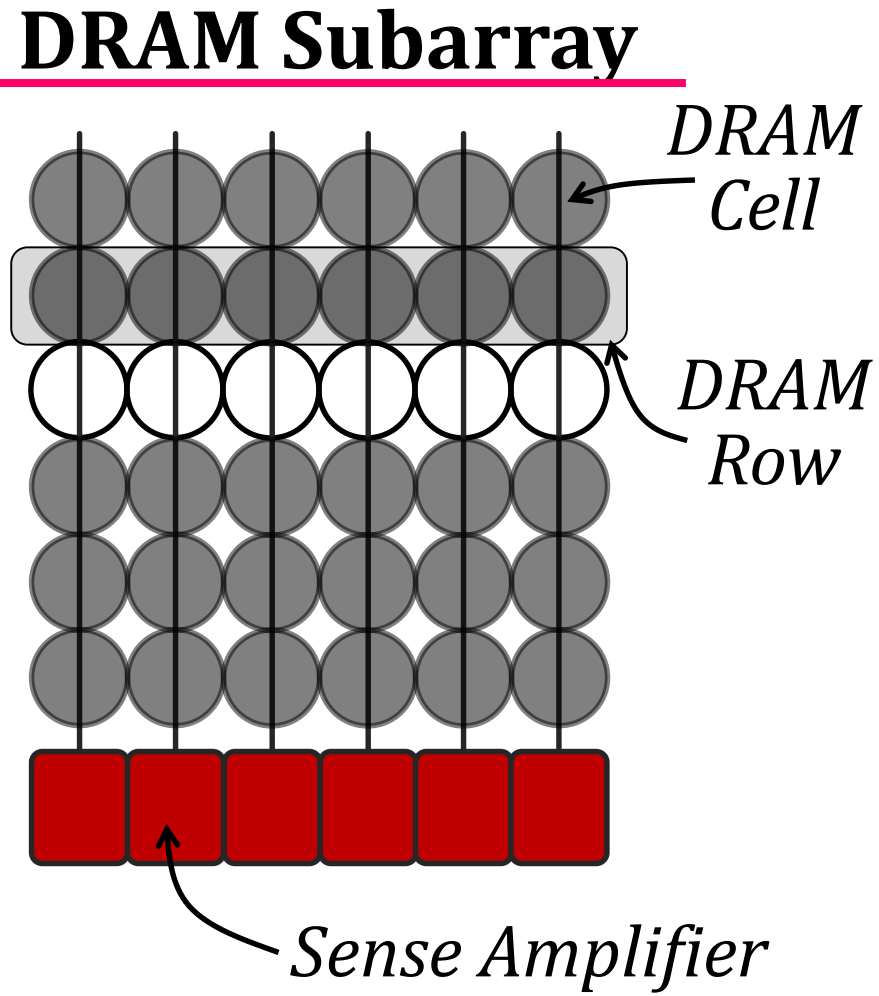

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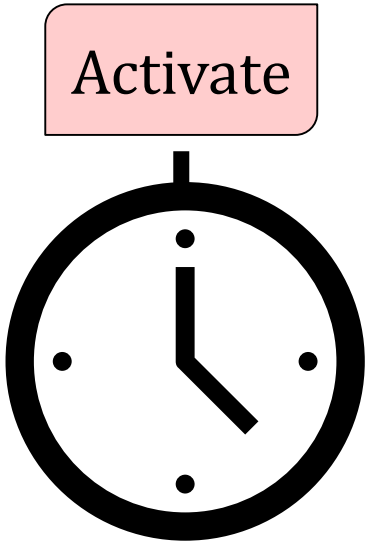

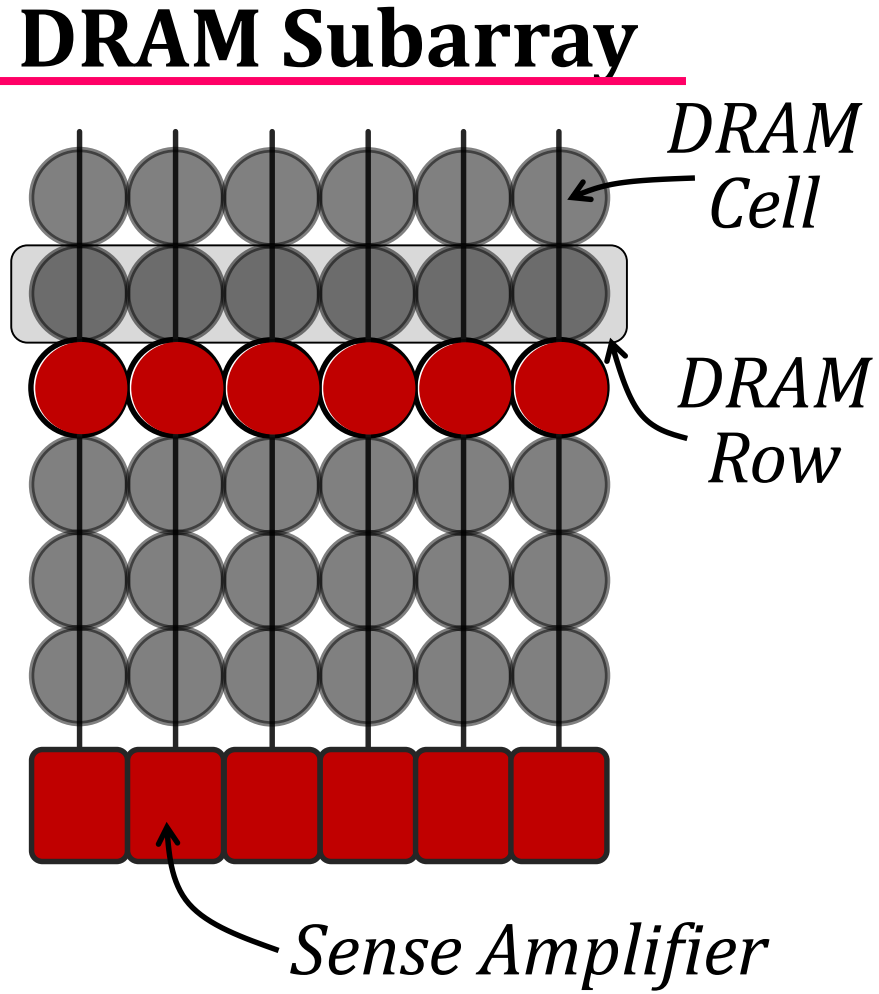

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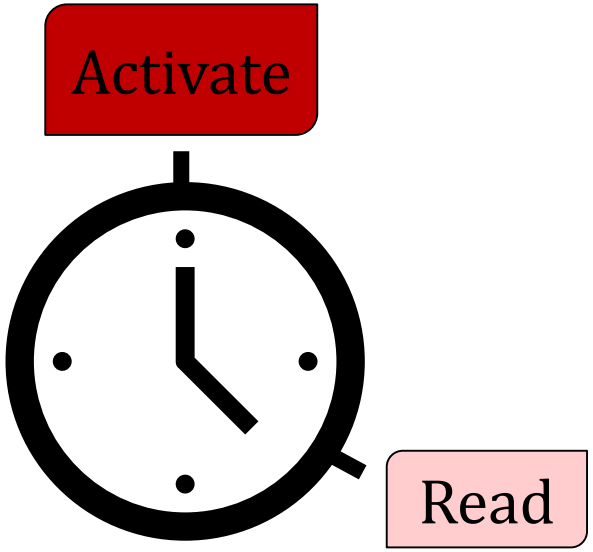

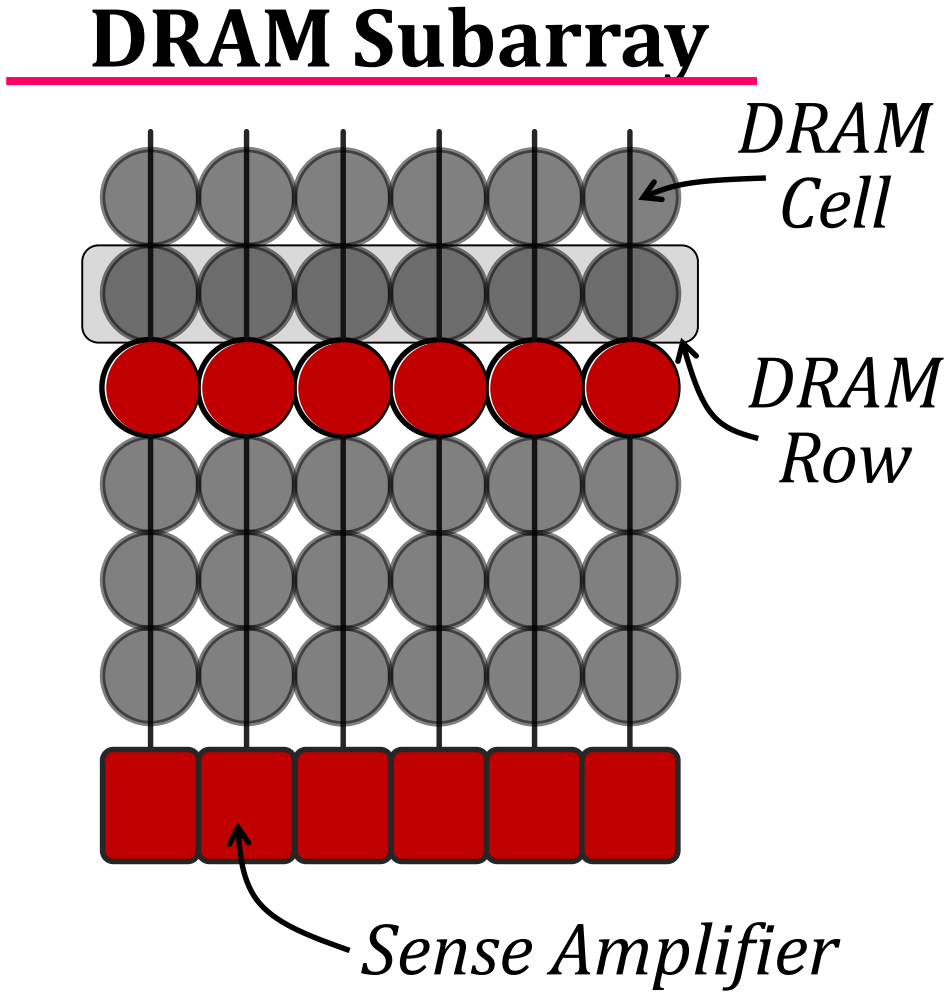

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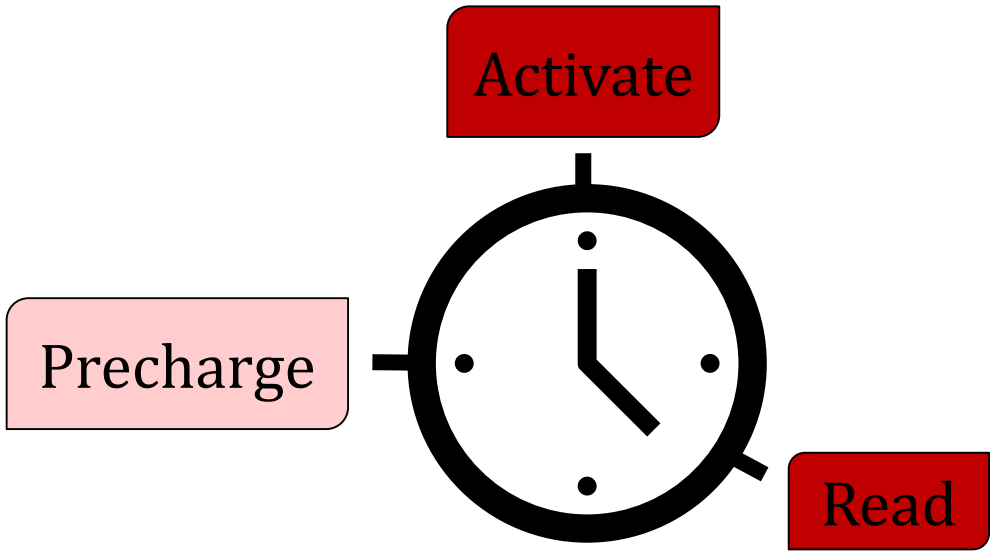

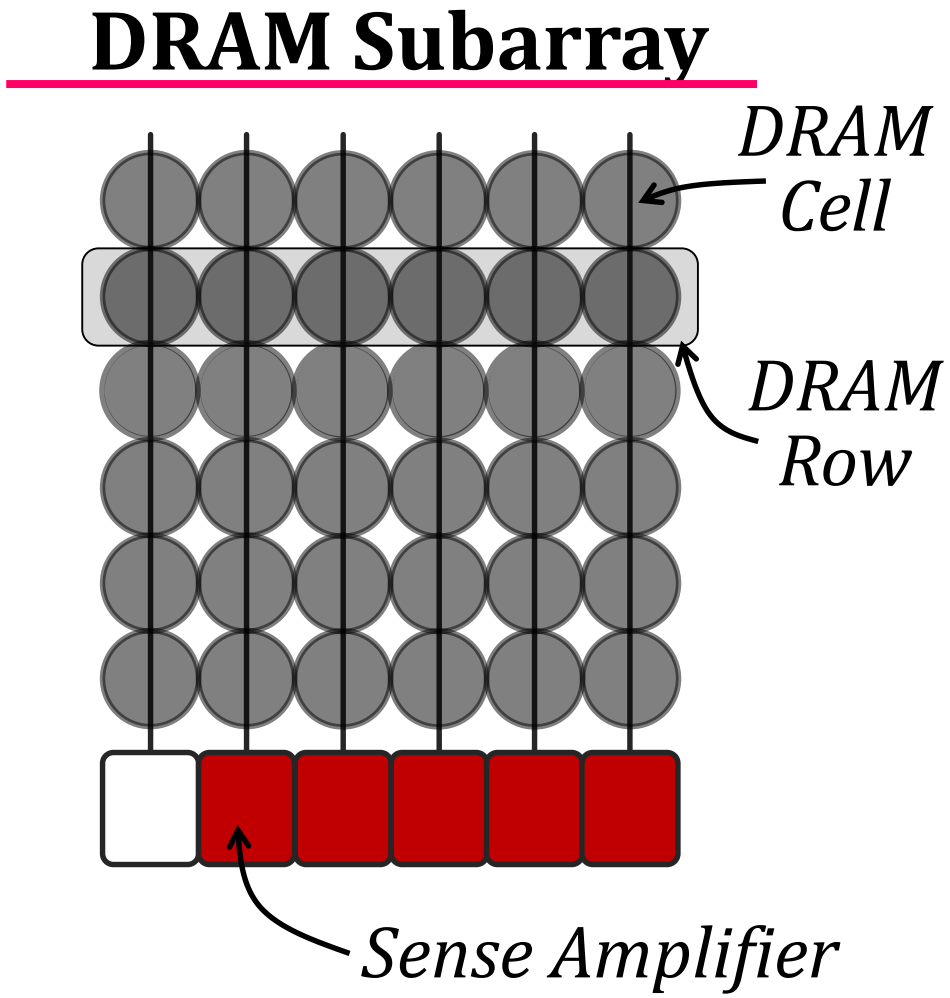

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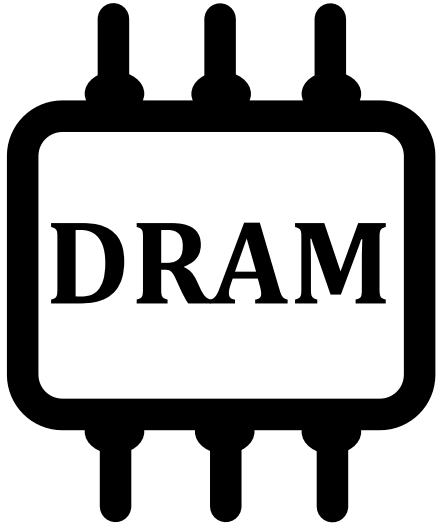

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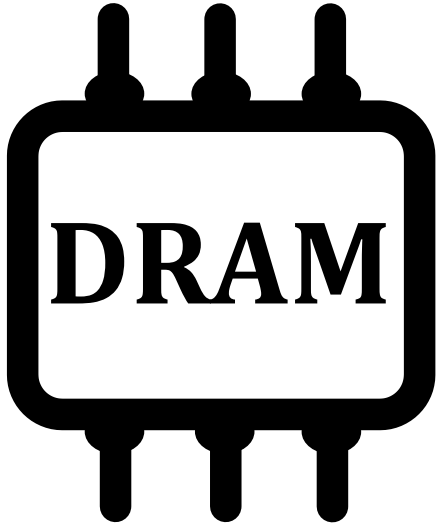

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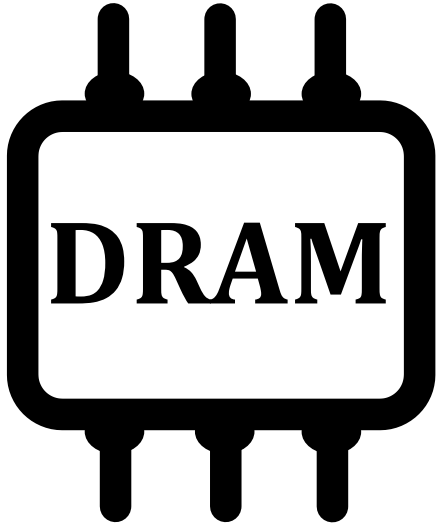

1. access latency

2. refresh overhead

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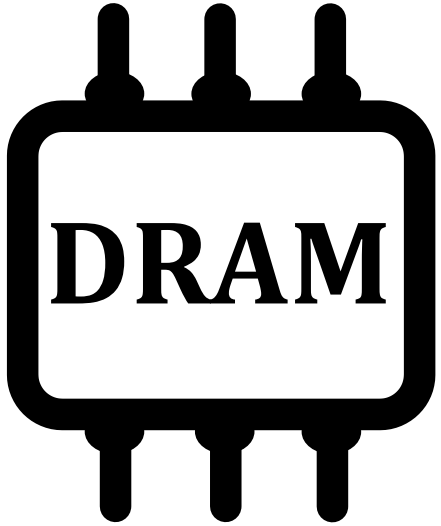

1. access latency
2. refresh overhead
3. exposure to vulnerabilities

Our Goal

We want a **substrate** that enables
the **duplication** and **remapping** of data within a subarray

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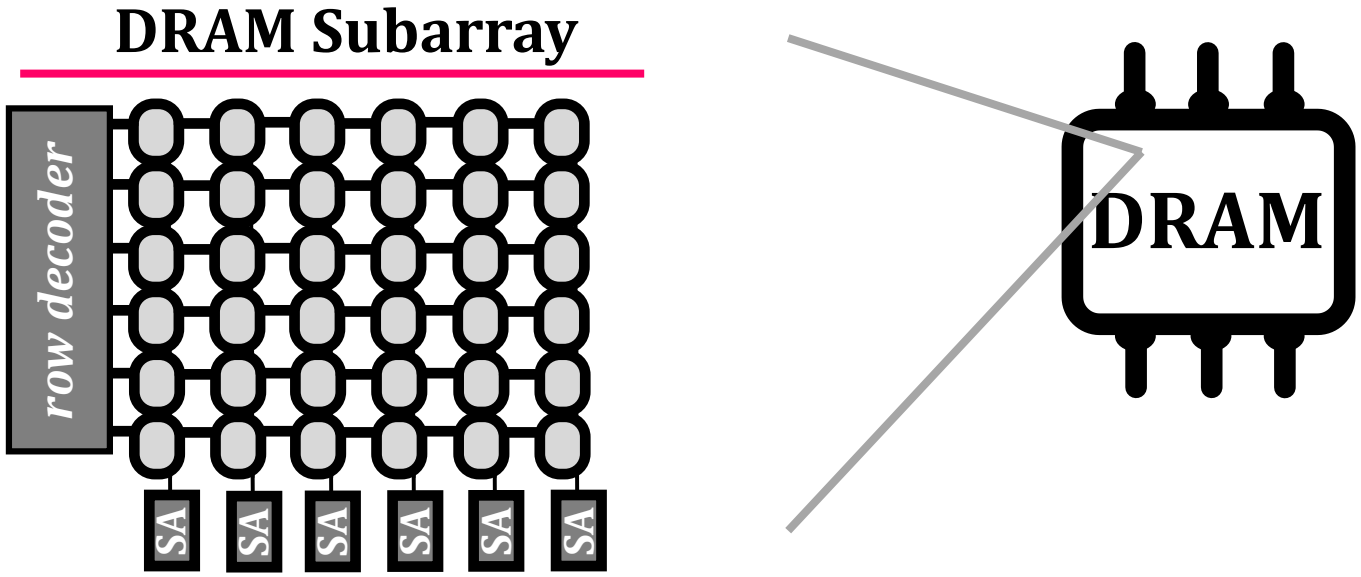

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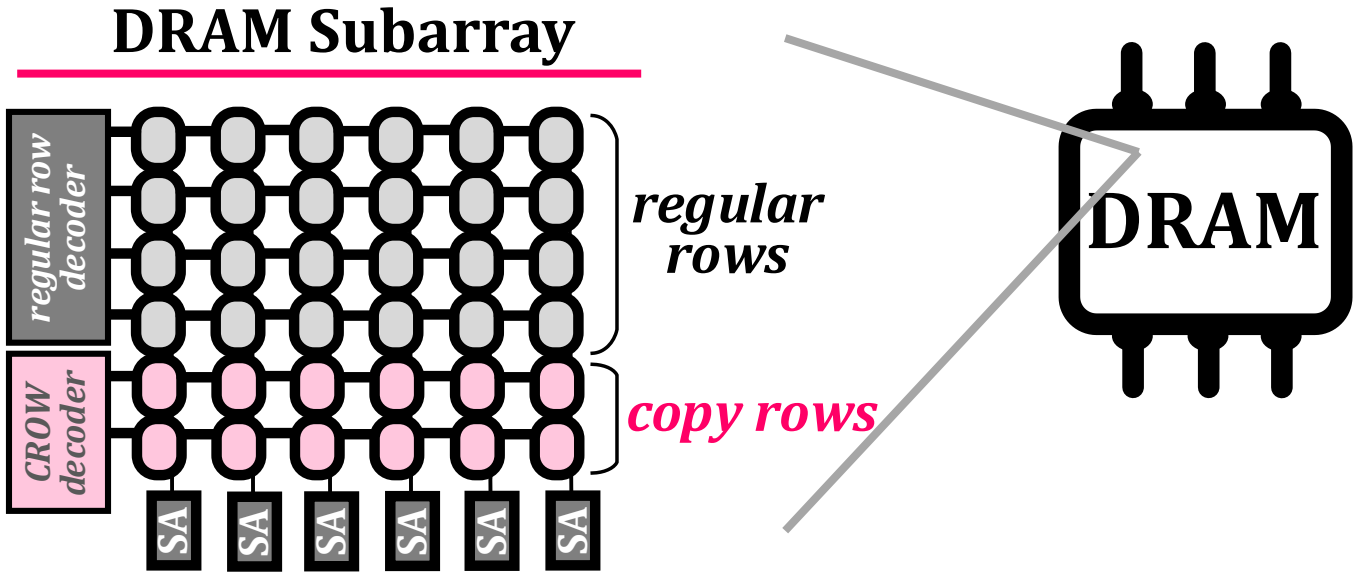

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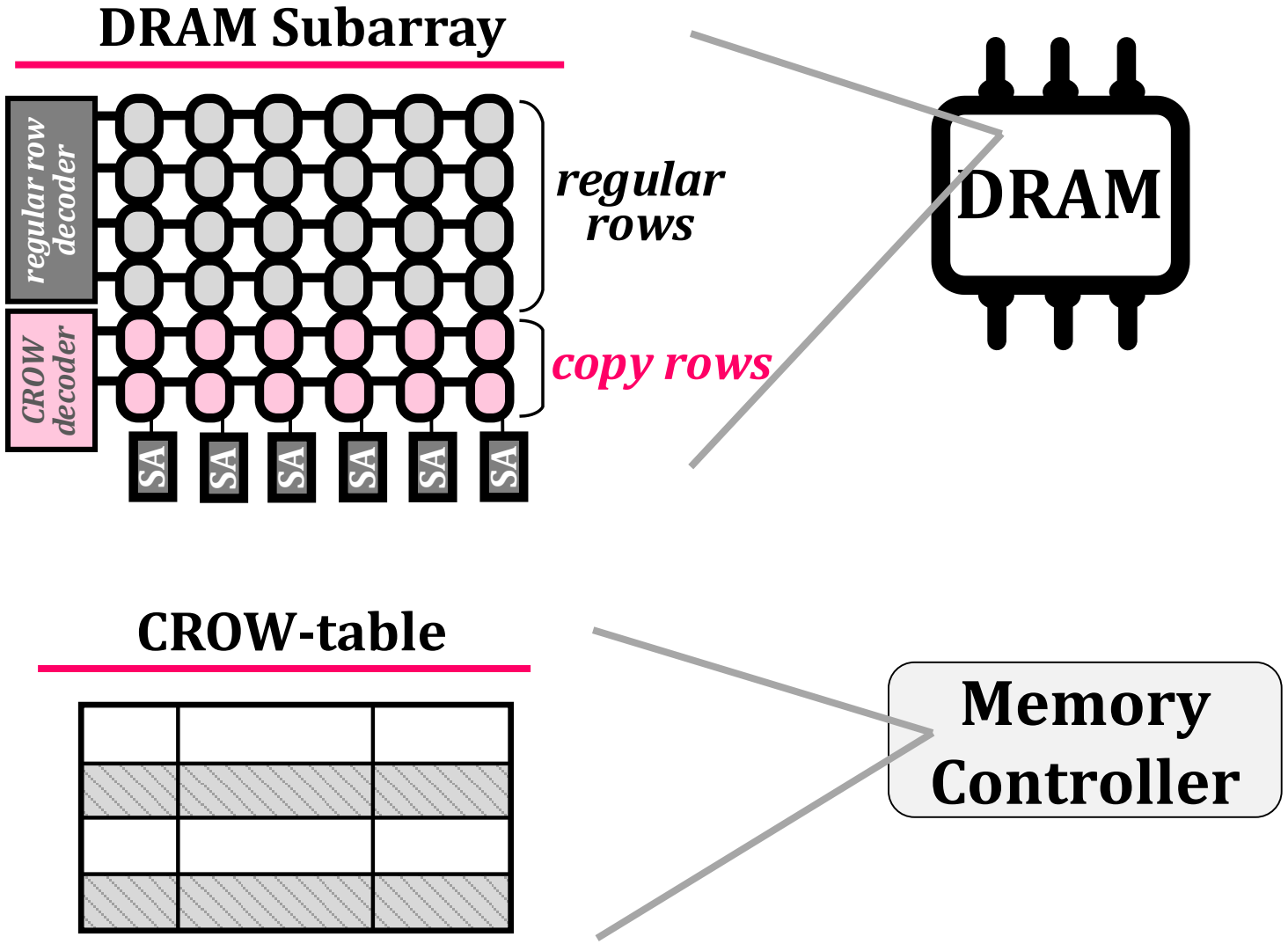
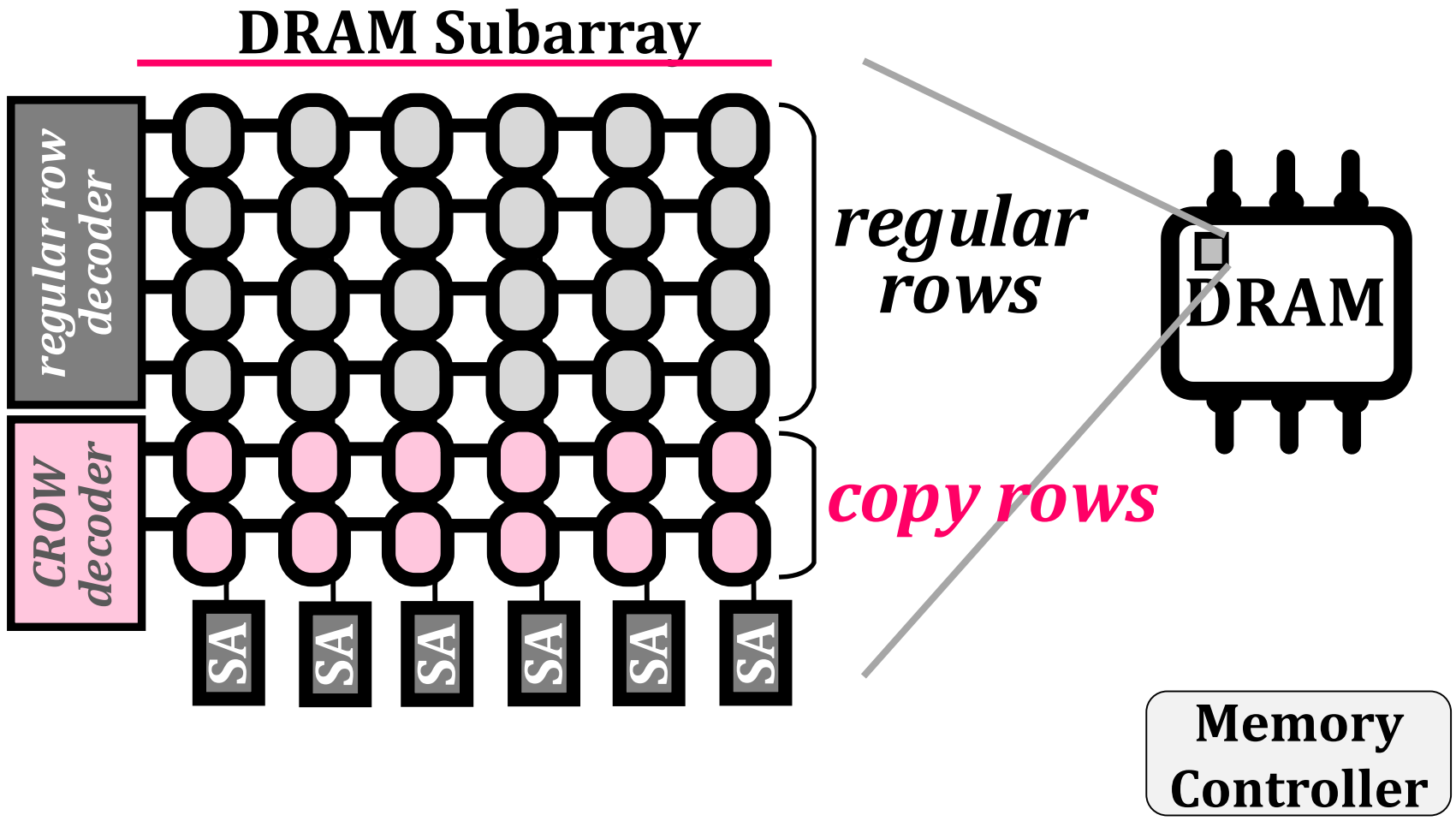


CROW Operation 1: Row Copy



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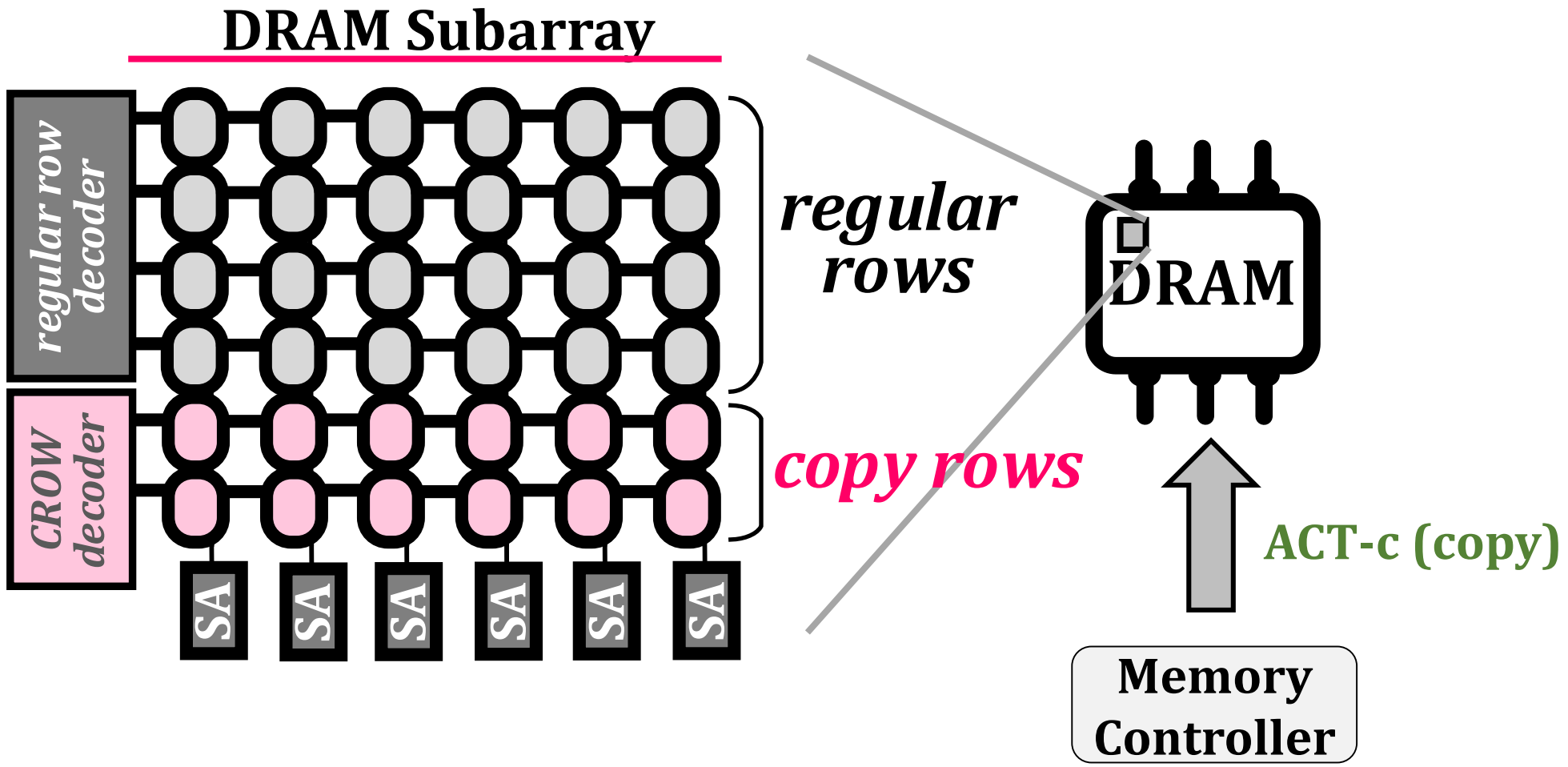

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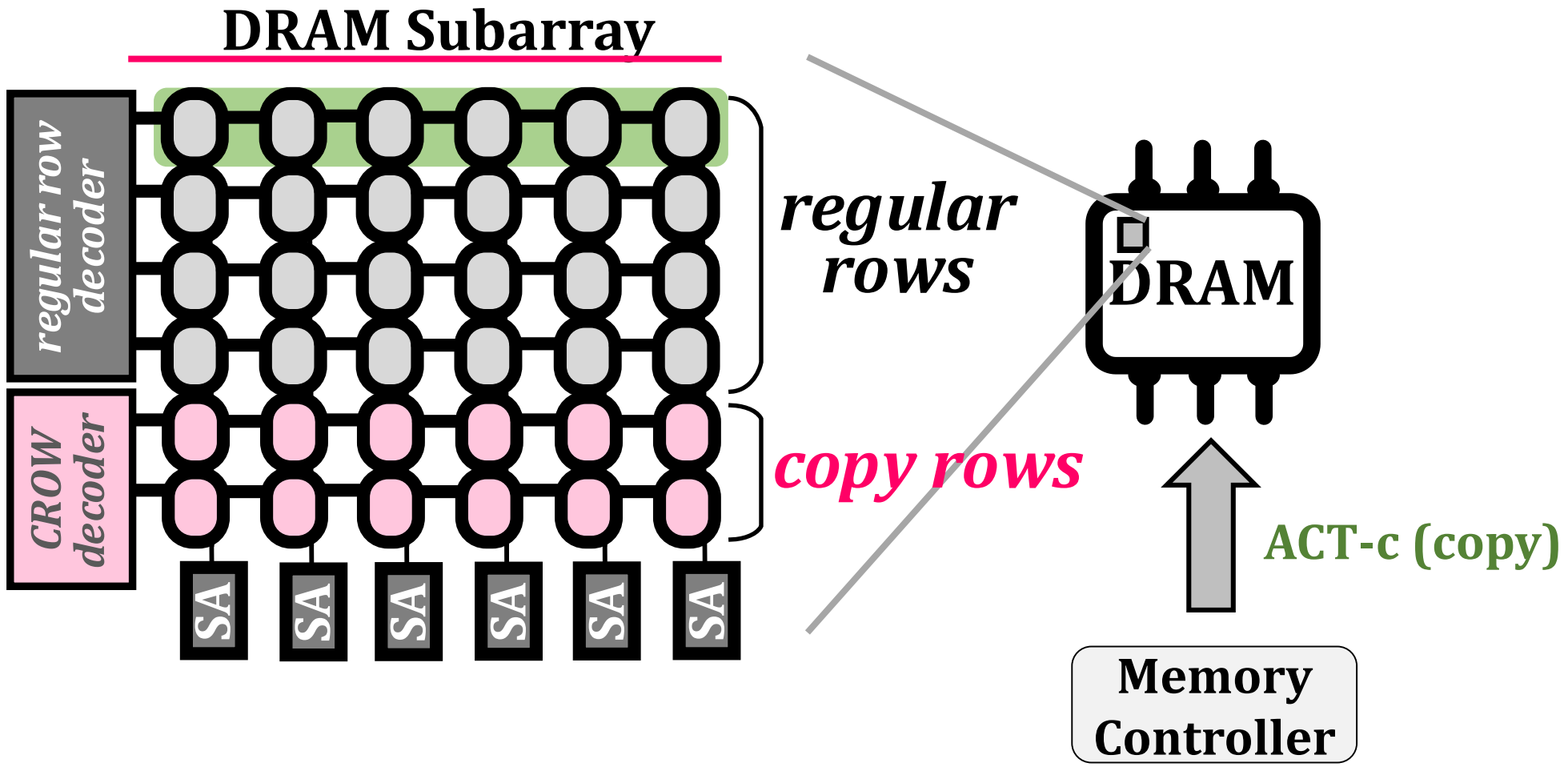

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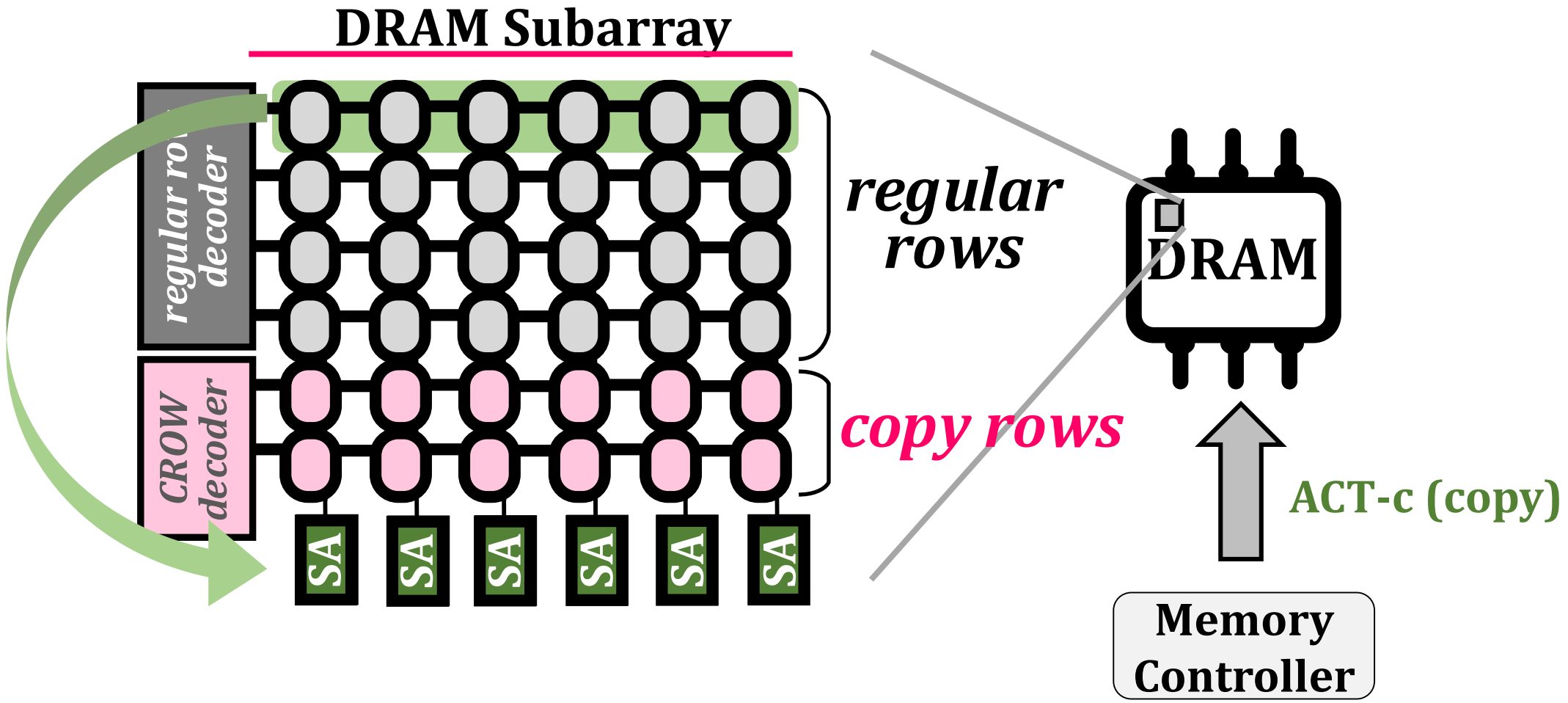

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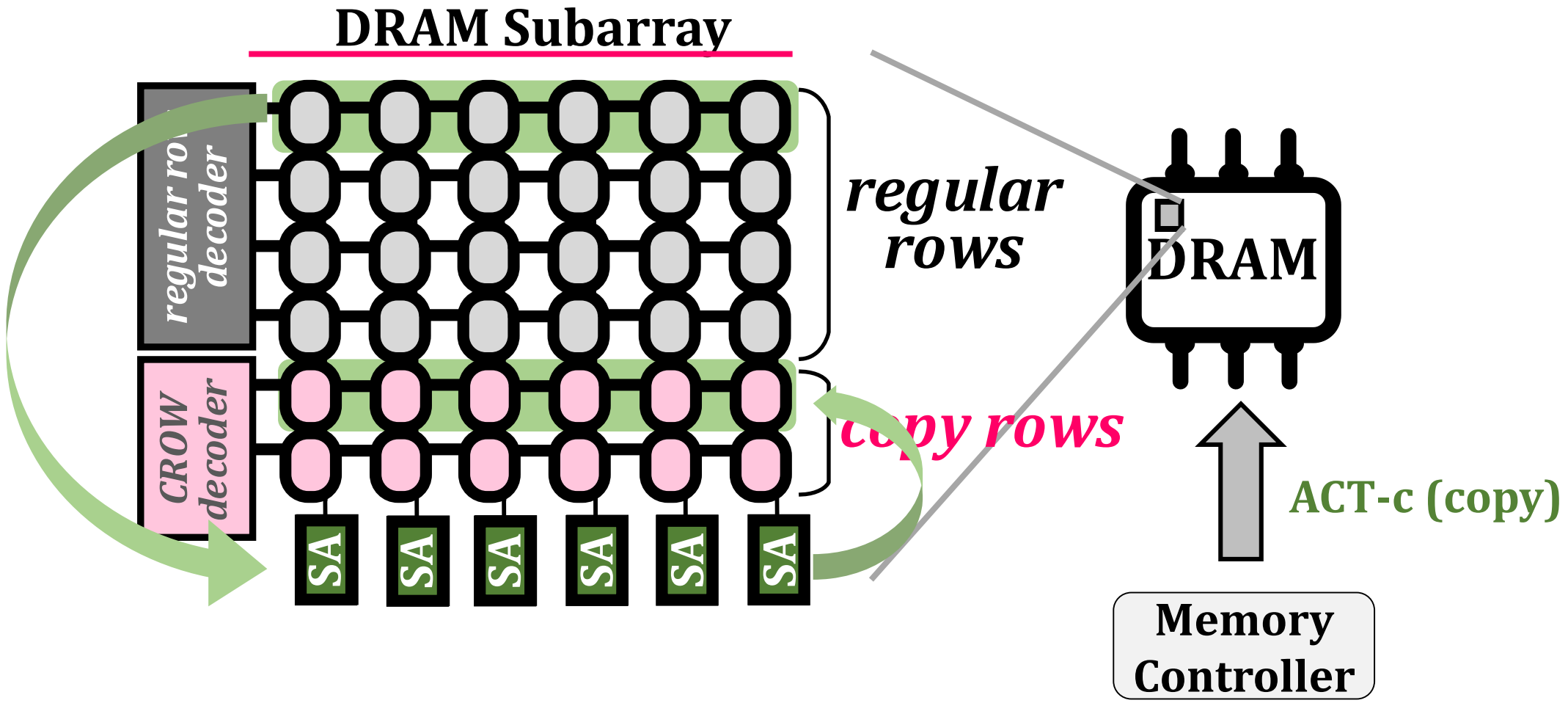

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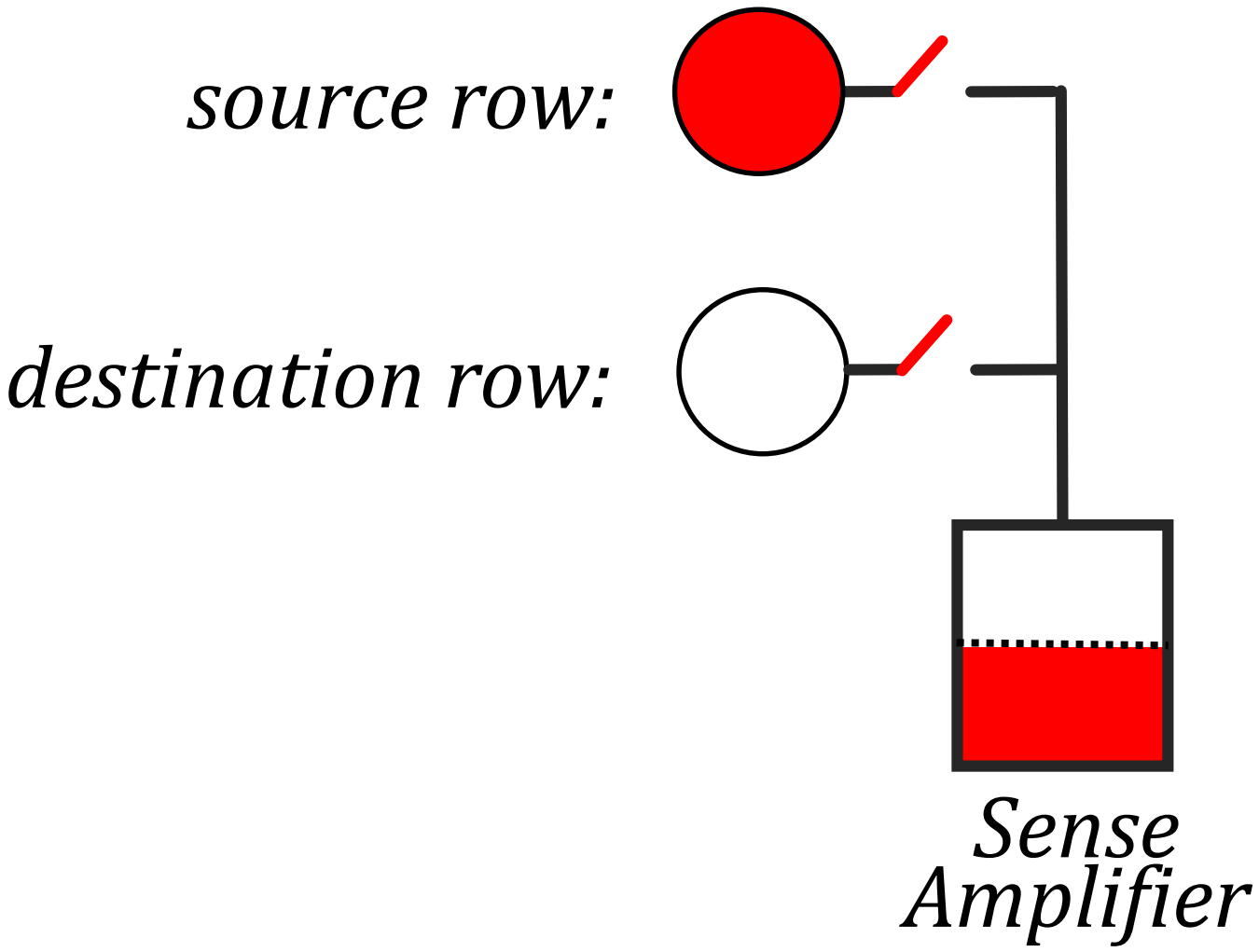

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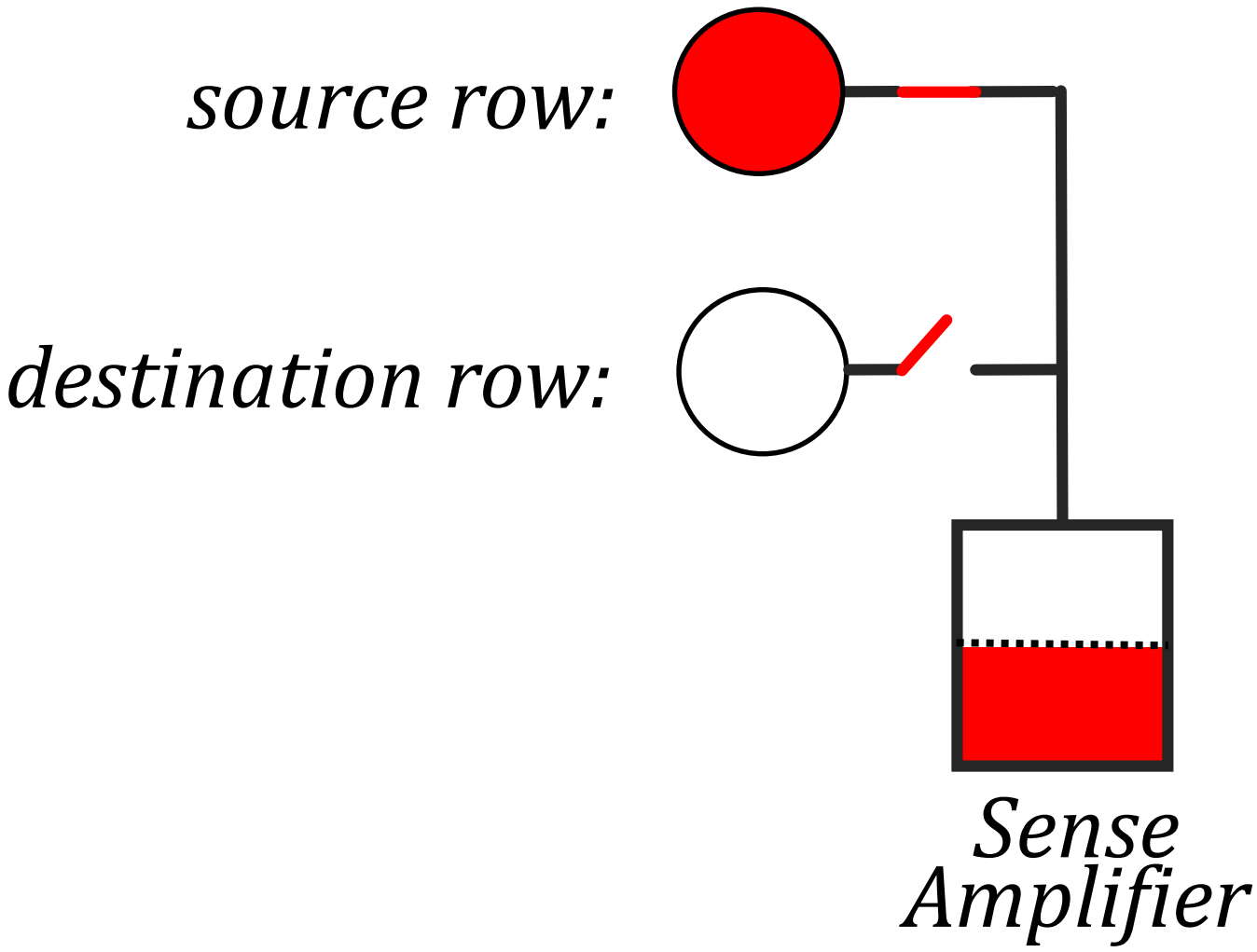
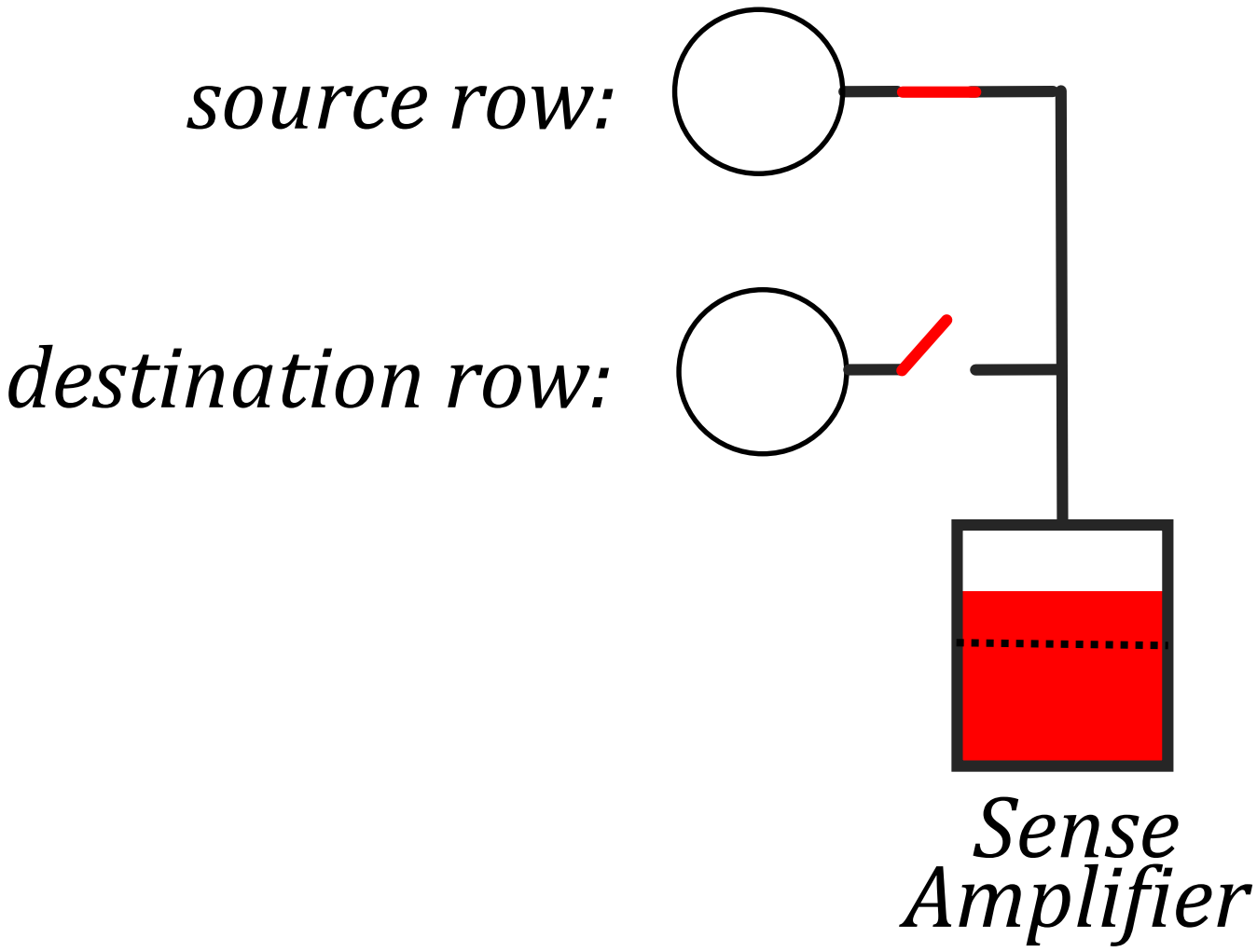


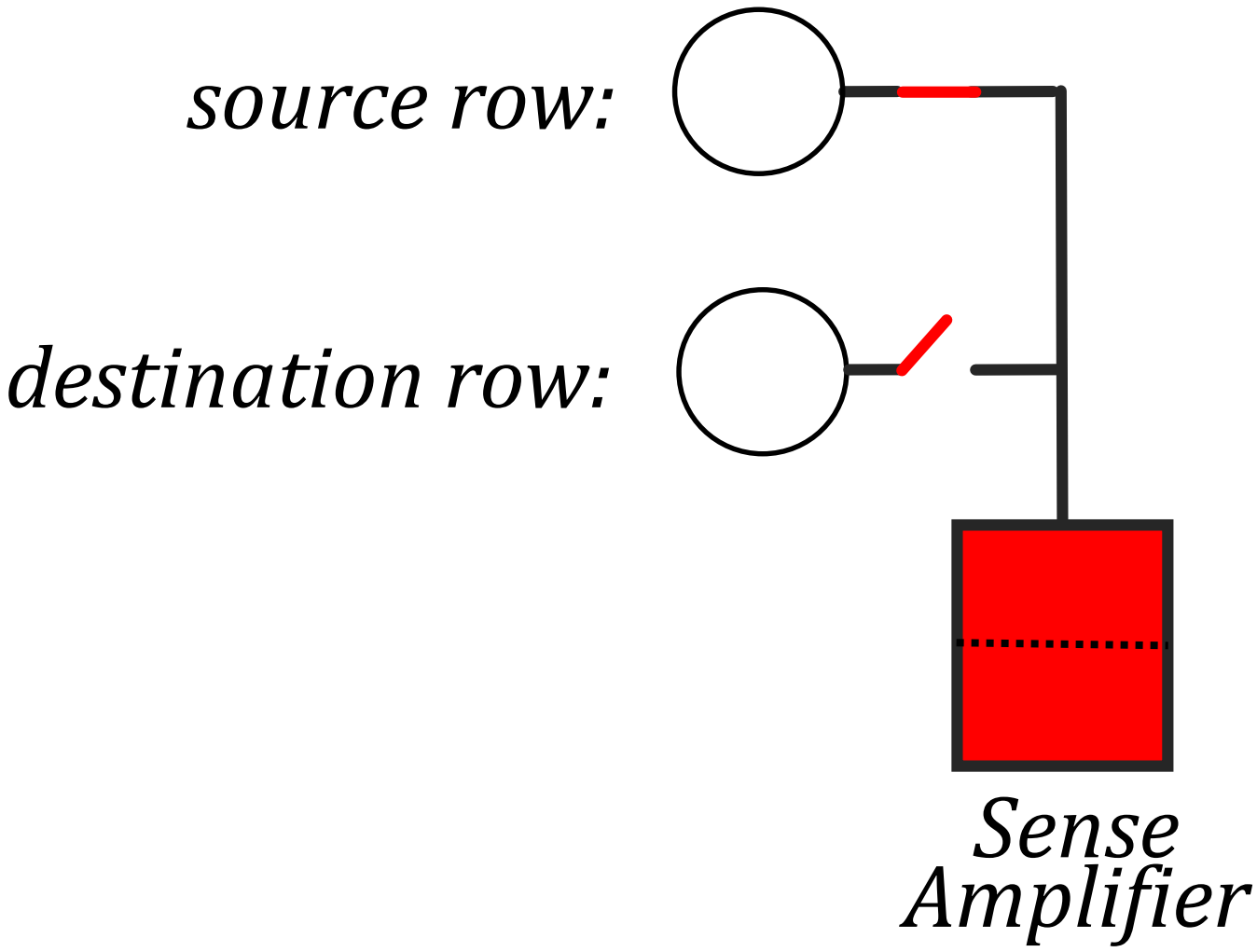
1. Activation of the source row

Row Copy: Steps



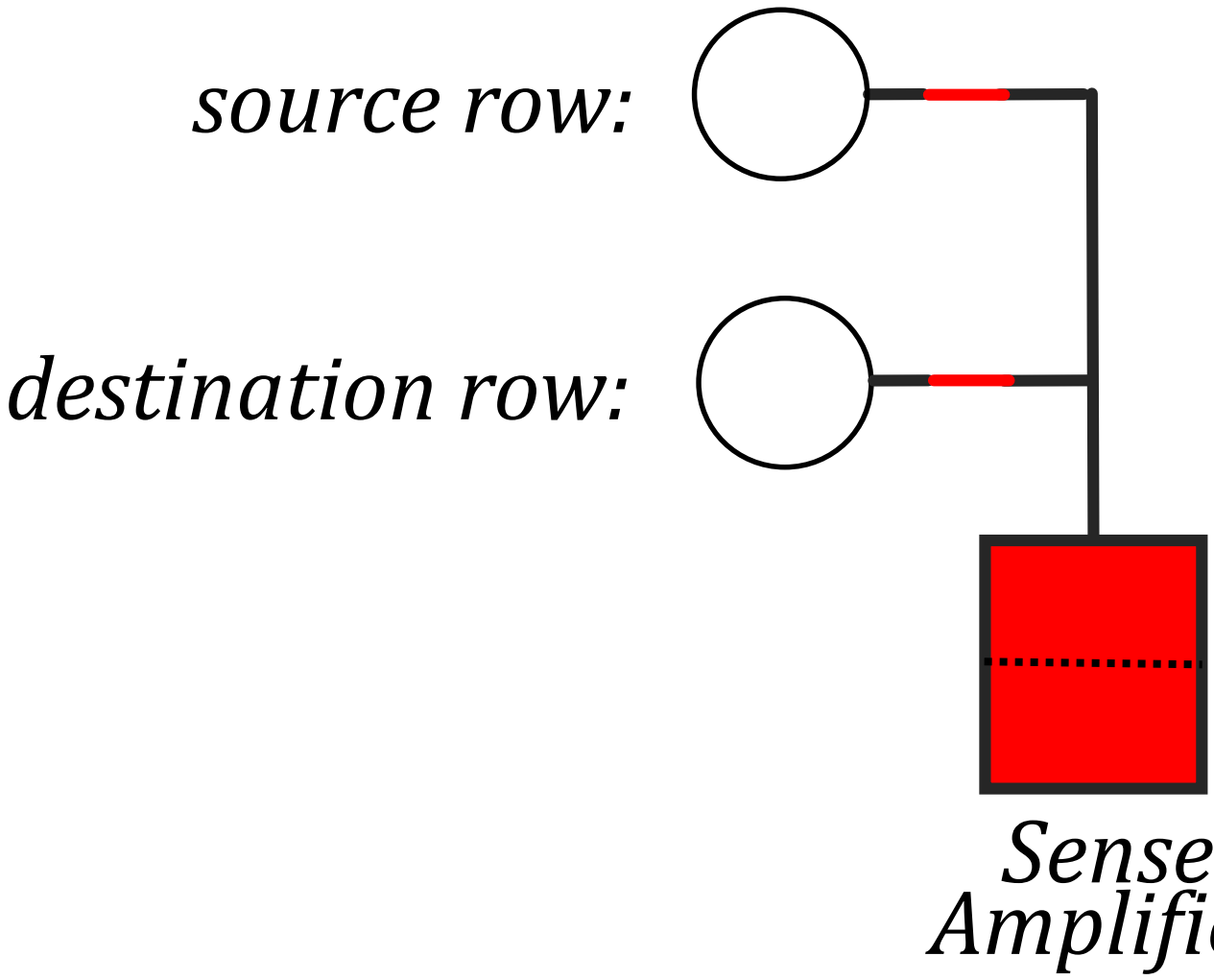
1. Activation of the source row
2. Charge sharing

Row Copy: Steps



1. Activation of the source row
2. Charge sharing
3. Beginning of restoration

Row Copy: Steps



1. Activation of the source row
2. Charge sharing
3. Beginning of restoration
4. Activation of the destination row

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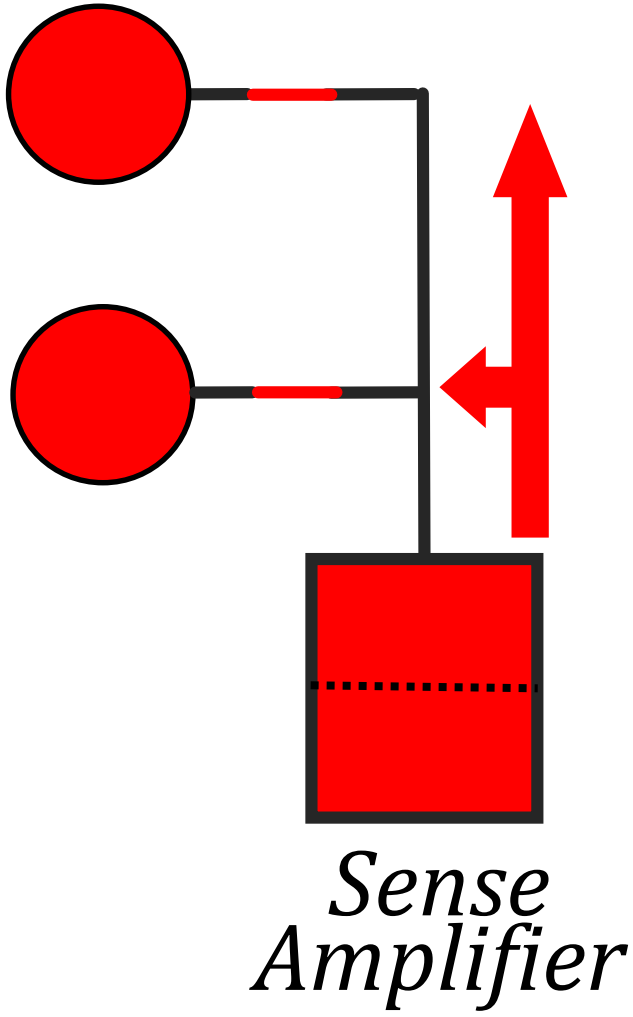

1. Activation of the source row
2. Charge sharing
3. Beginning of restoration
4. Activation of the destination row
5. Restoration of both rows to source data

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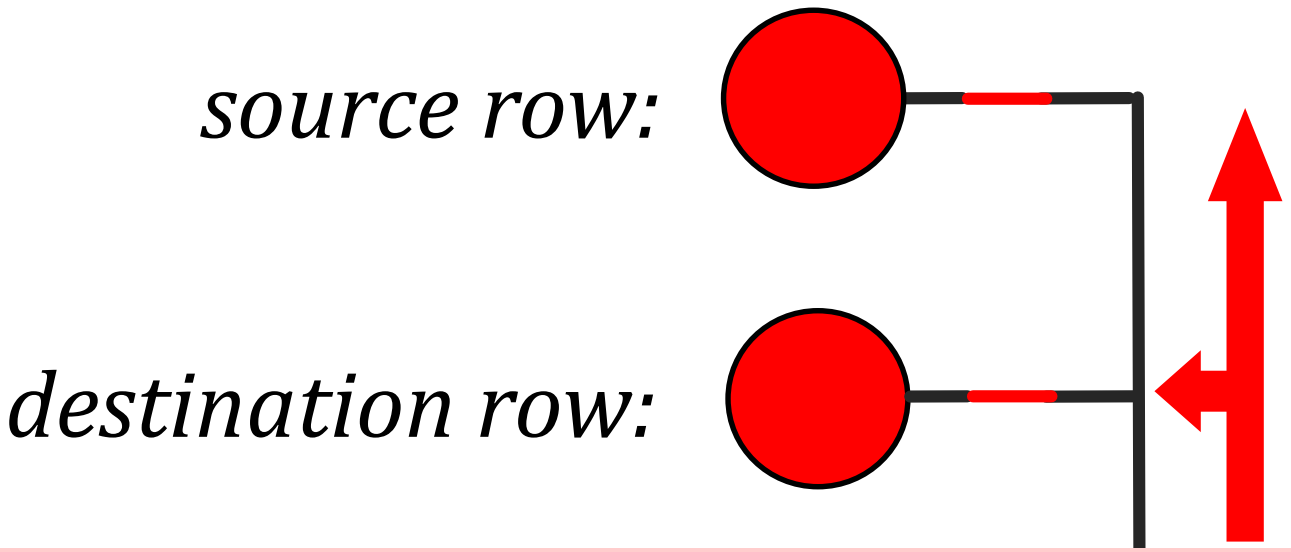
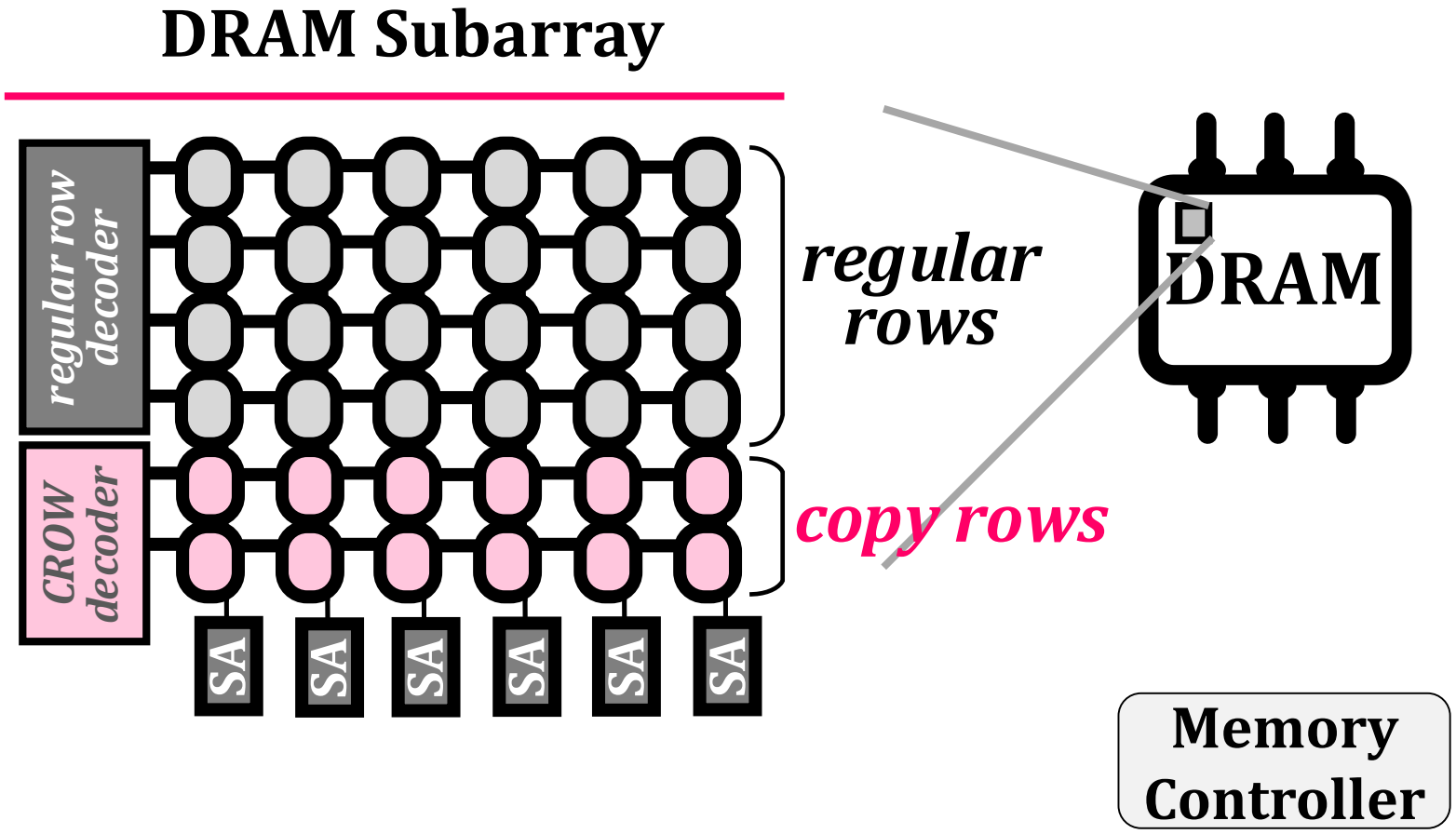


1. Activation of the source row
2. Charge sharing
3. Beginning of restoration

Enables quickly copying a regular row into a copy row

Amplifier

CROW Operation 2: Two-Row Activation



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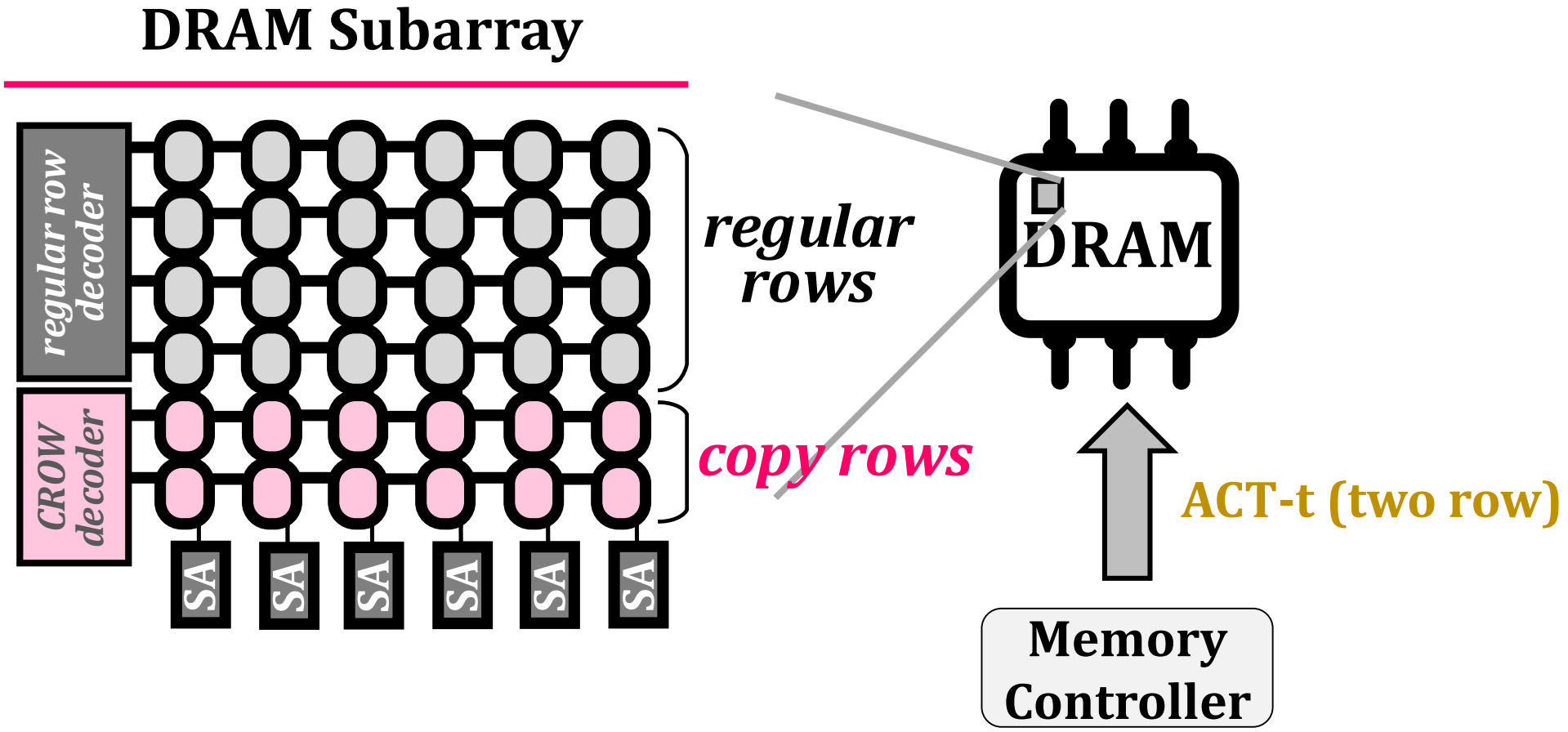
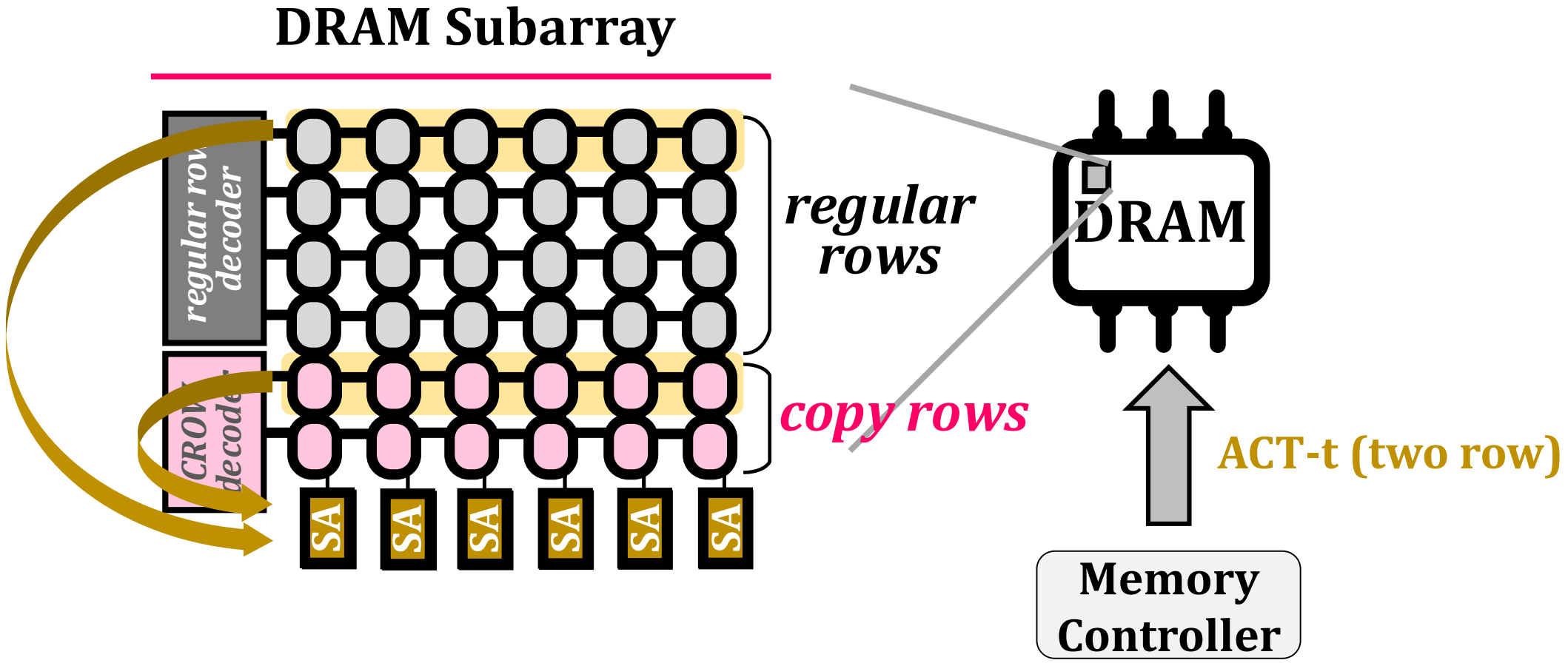
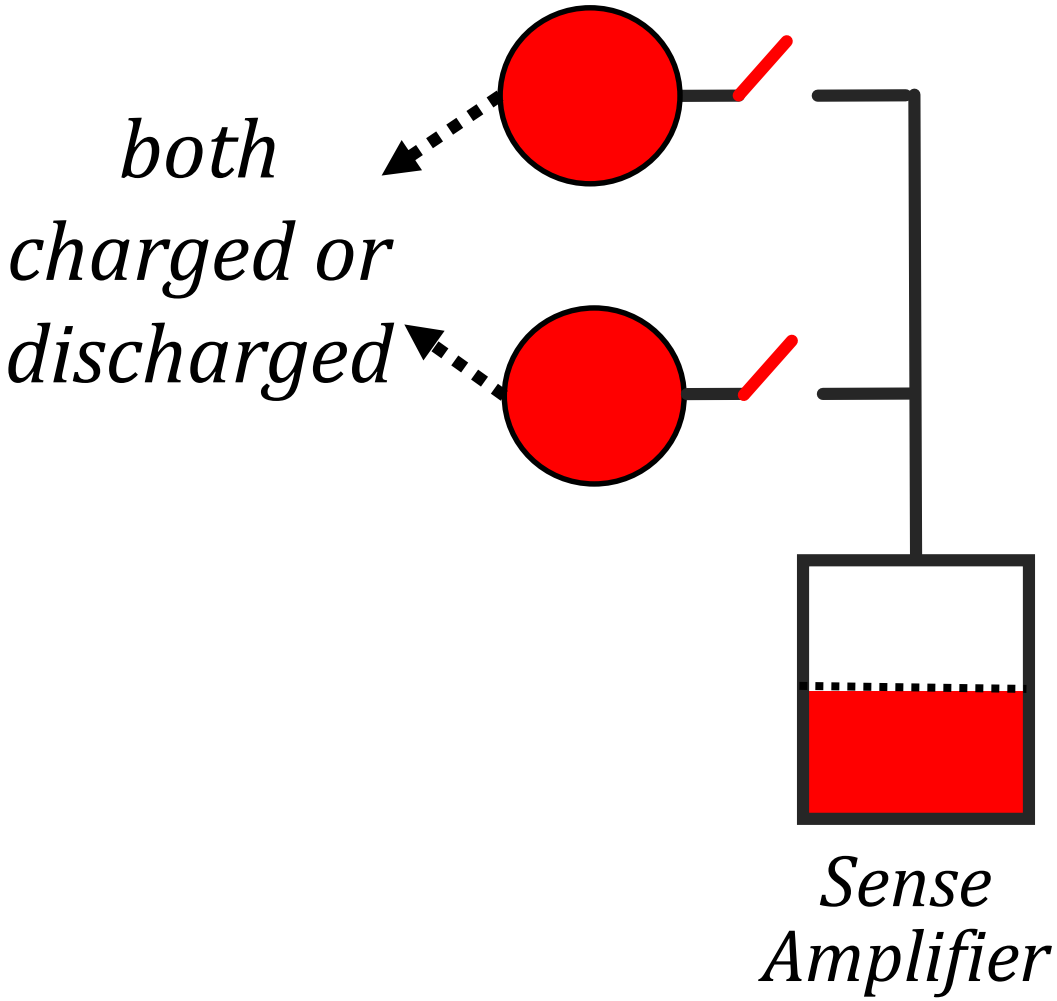


CROW Operation 2: Two-Row Activation



Two-Row Activation: Steps



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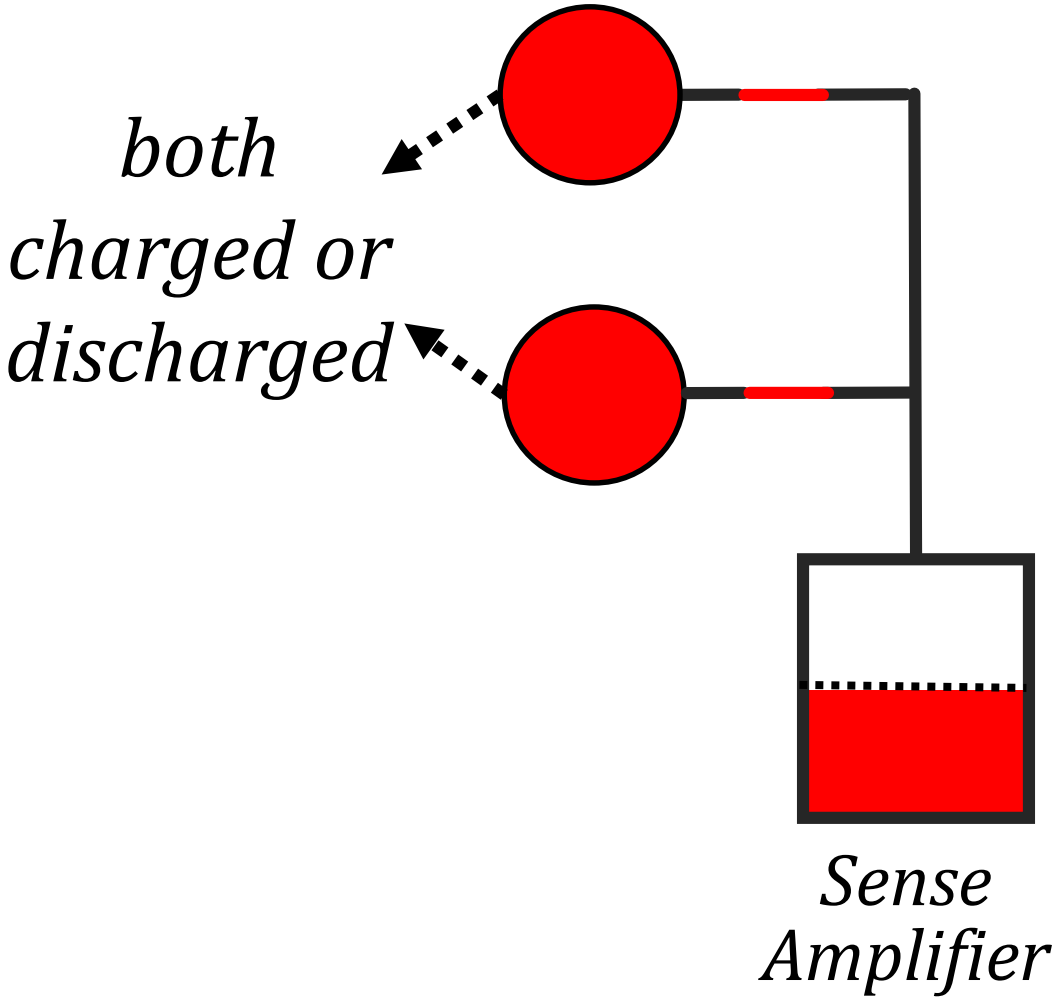
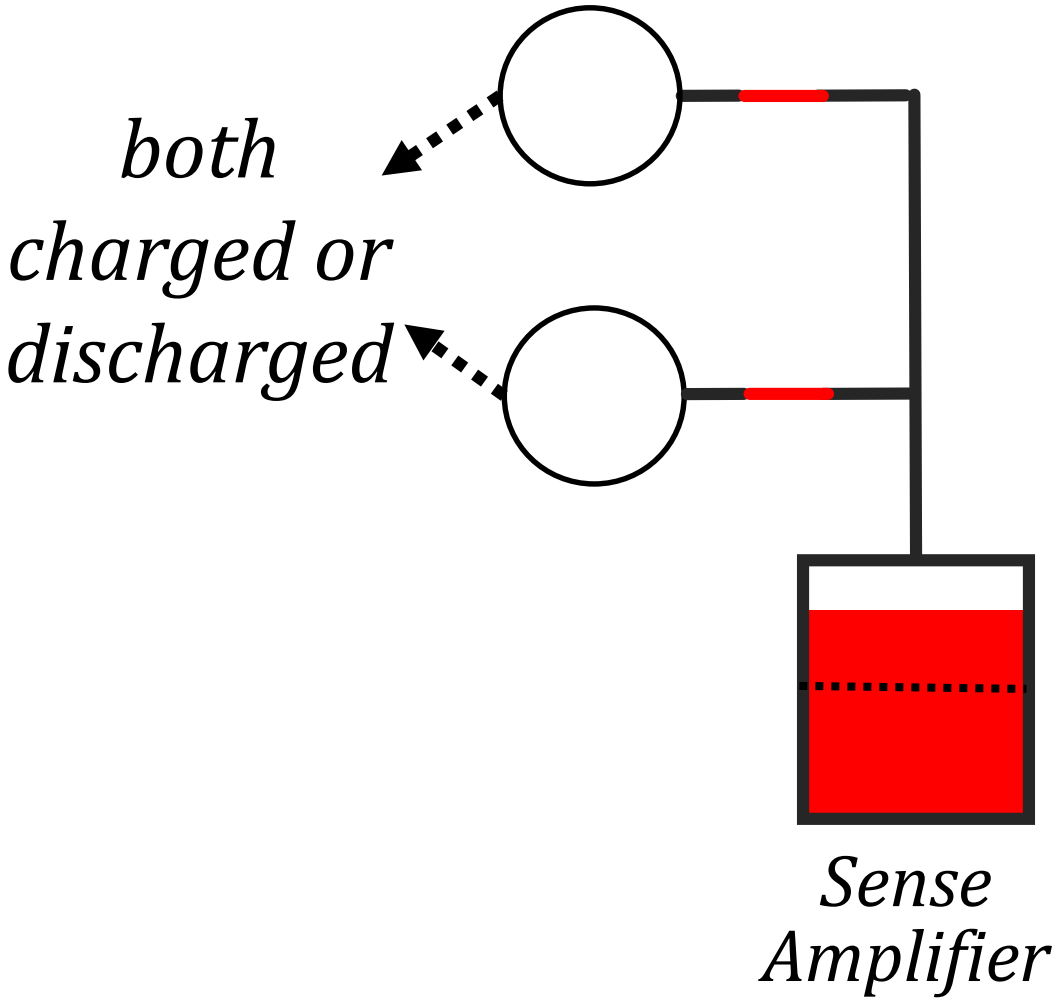


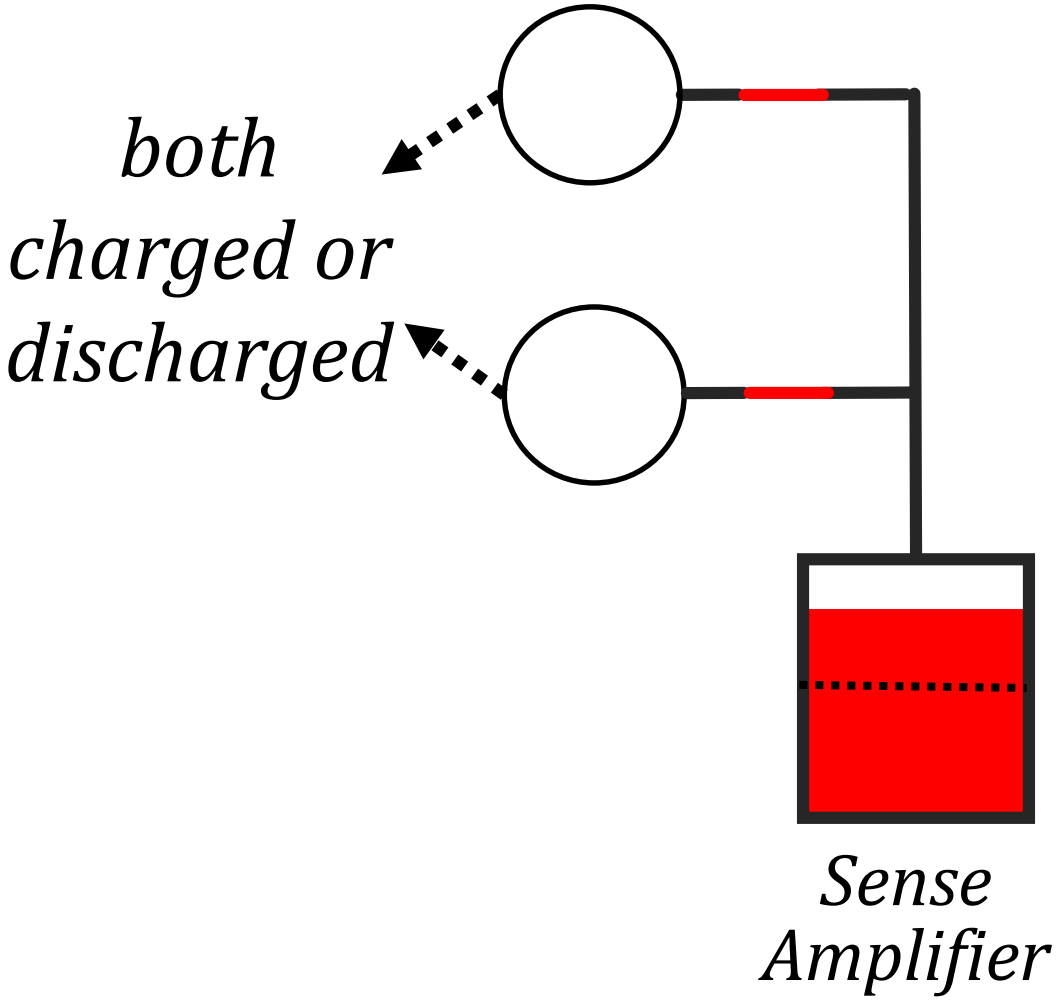
1. Activation of two rows

Two-Row Activation: Steps



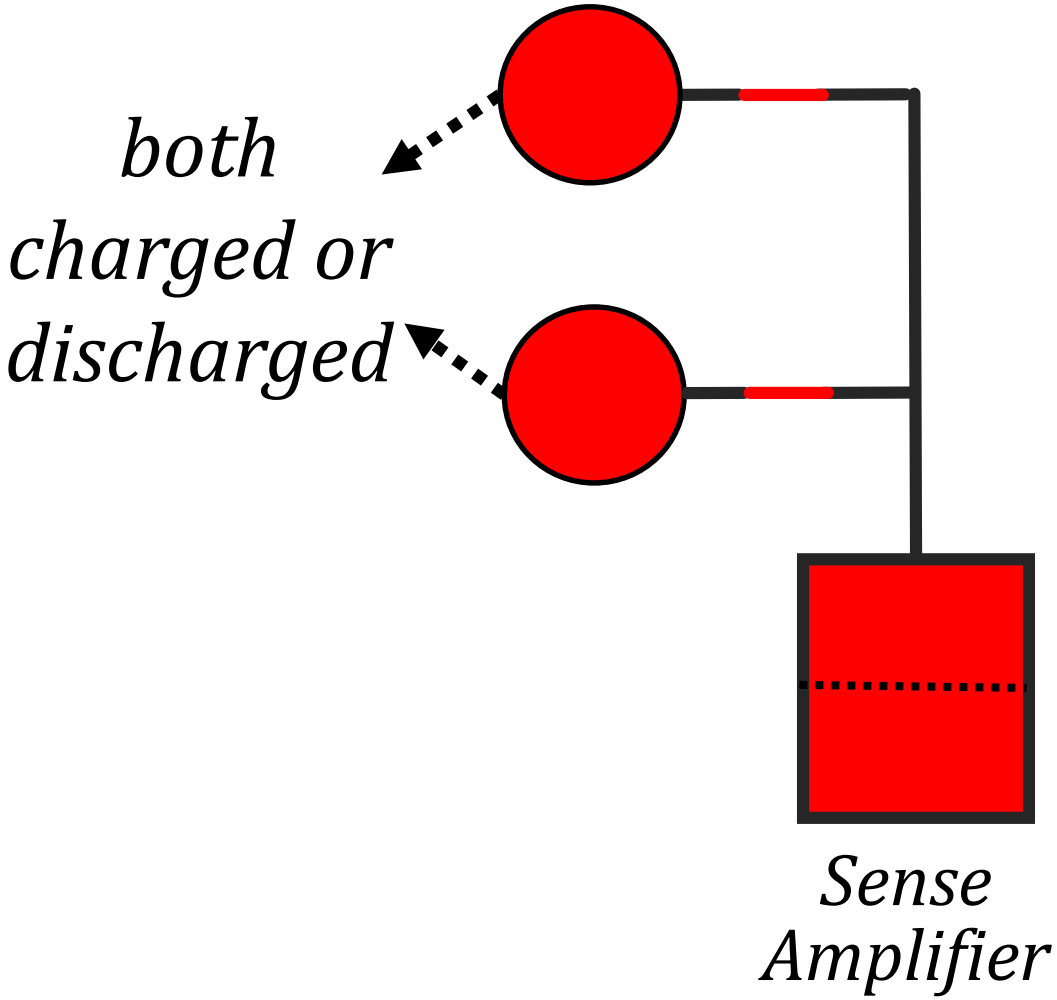
1. Activation of two rows
2. Charge sharing

Two-Row Activation: Steps



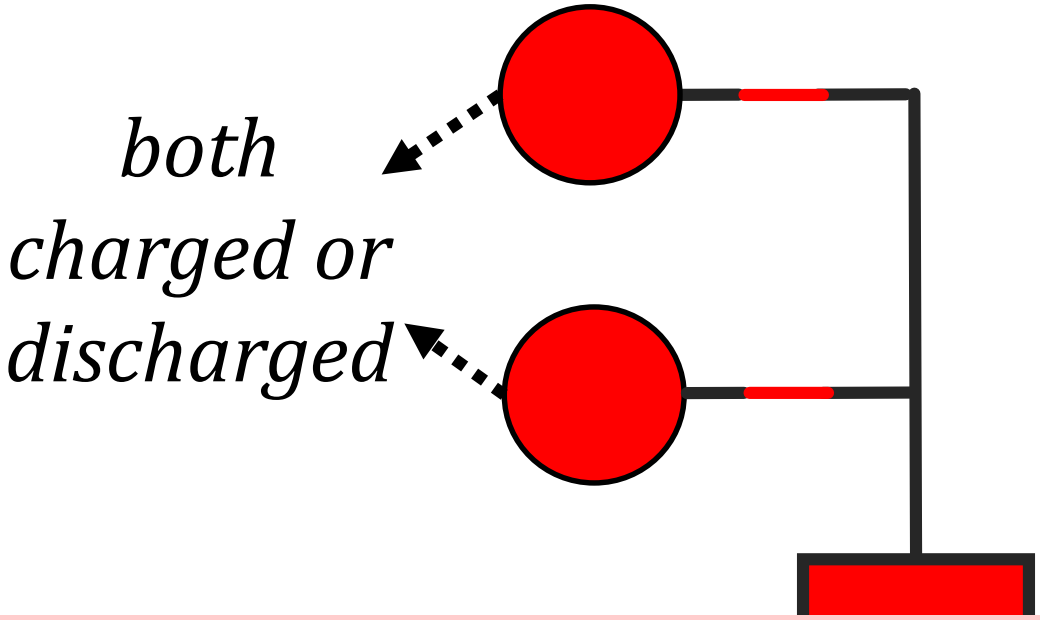
1. Activation of two rows
2. Charge sharing **fast**

Two-Row Activation: Steps



1. Activation of two rows
2. Charge sharing **fast**
3. Restoration

Two-Row Activation: Steps



1. Activation of two rows
2. Charge sharing **fast**

Enables fast access to data that is duplicated across a regular row and a copy row

Outline

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2. The CROW Substrate
   - CROW-cache: Reducing DRAM Latency
   - CROW-ref: Reducing DRAM Refresh
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CROW-cache

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Reduces activation latency by **38%**

CROW-cache Operation

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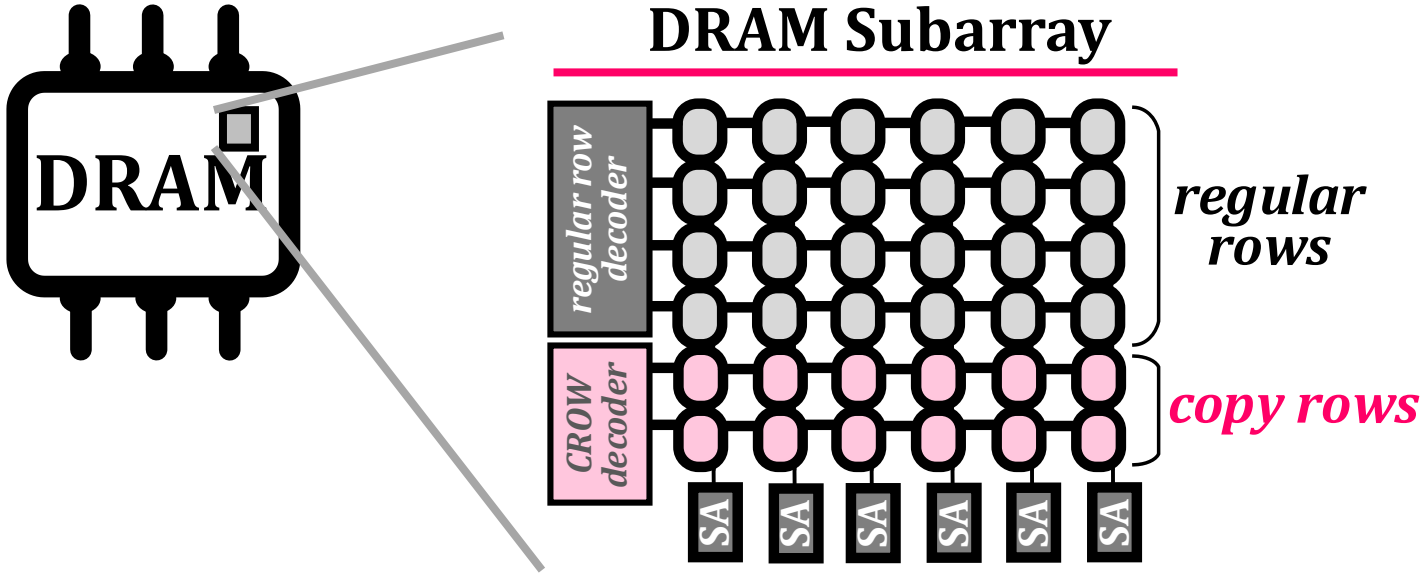

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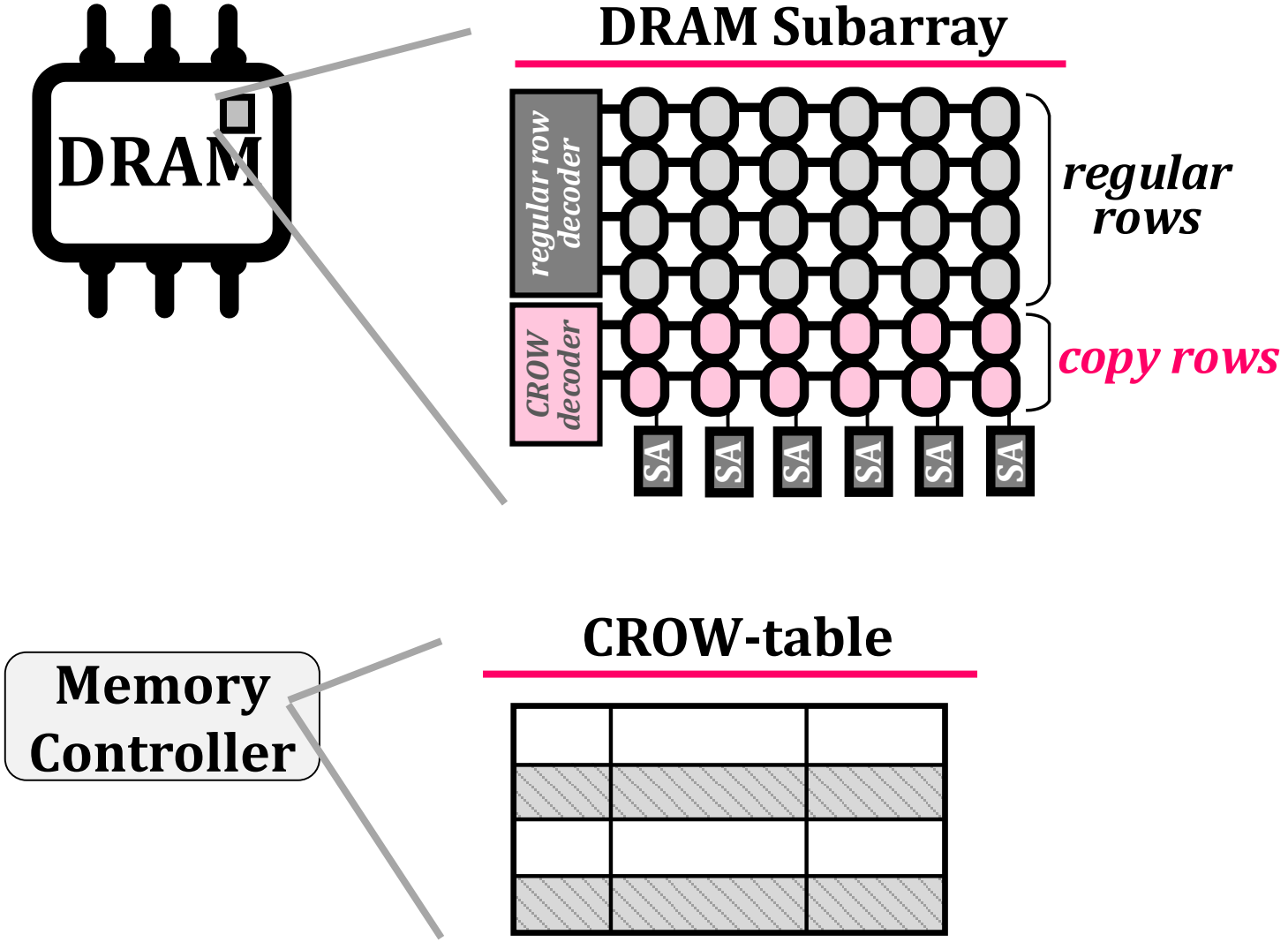
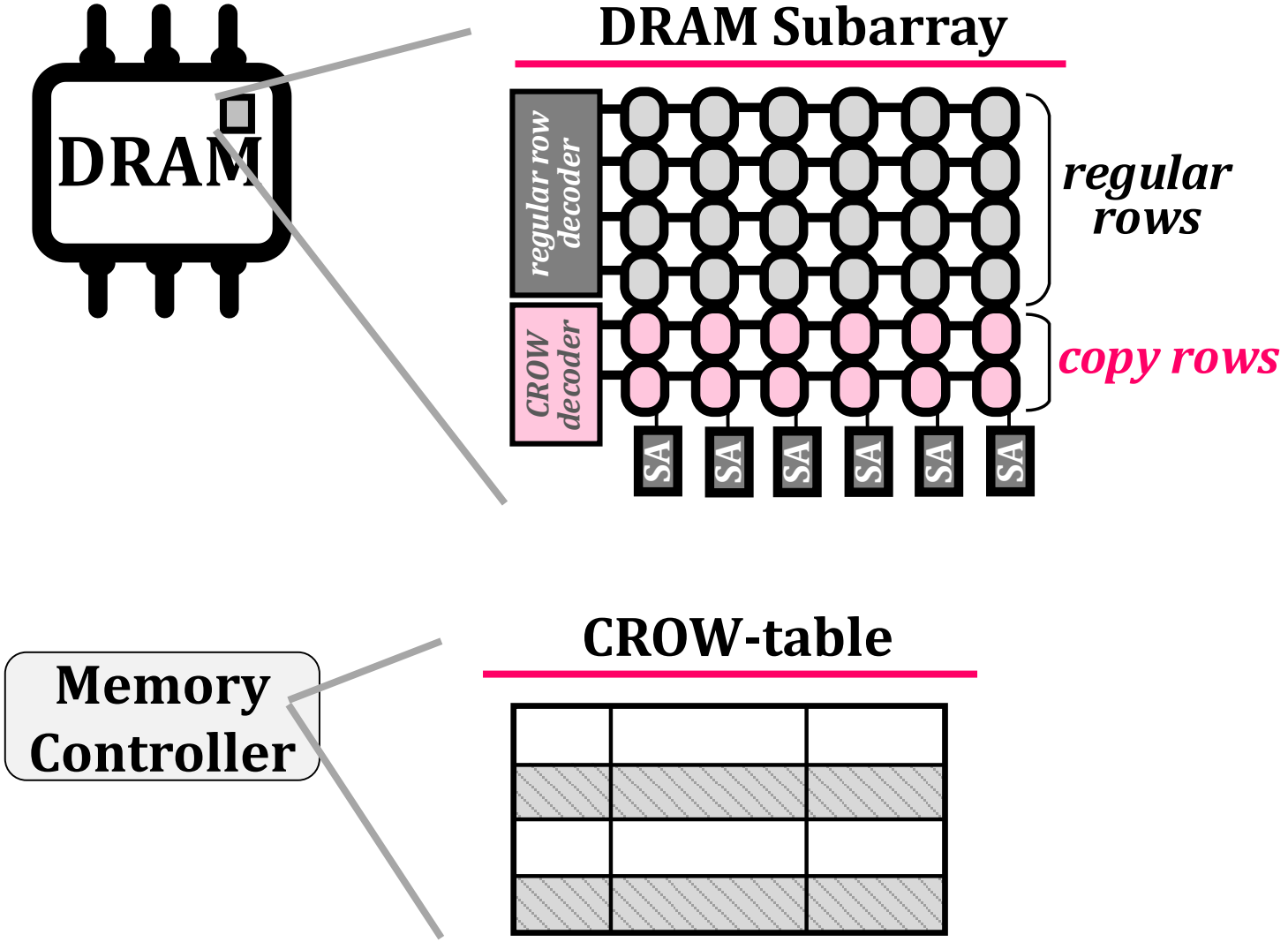


CROW-cache Operation

Request Queue



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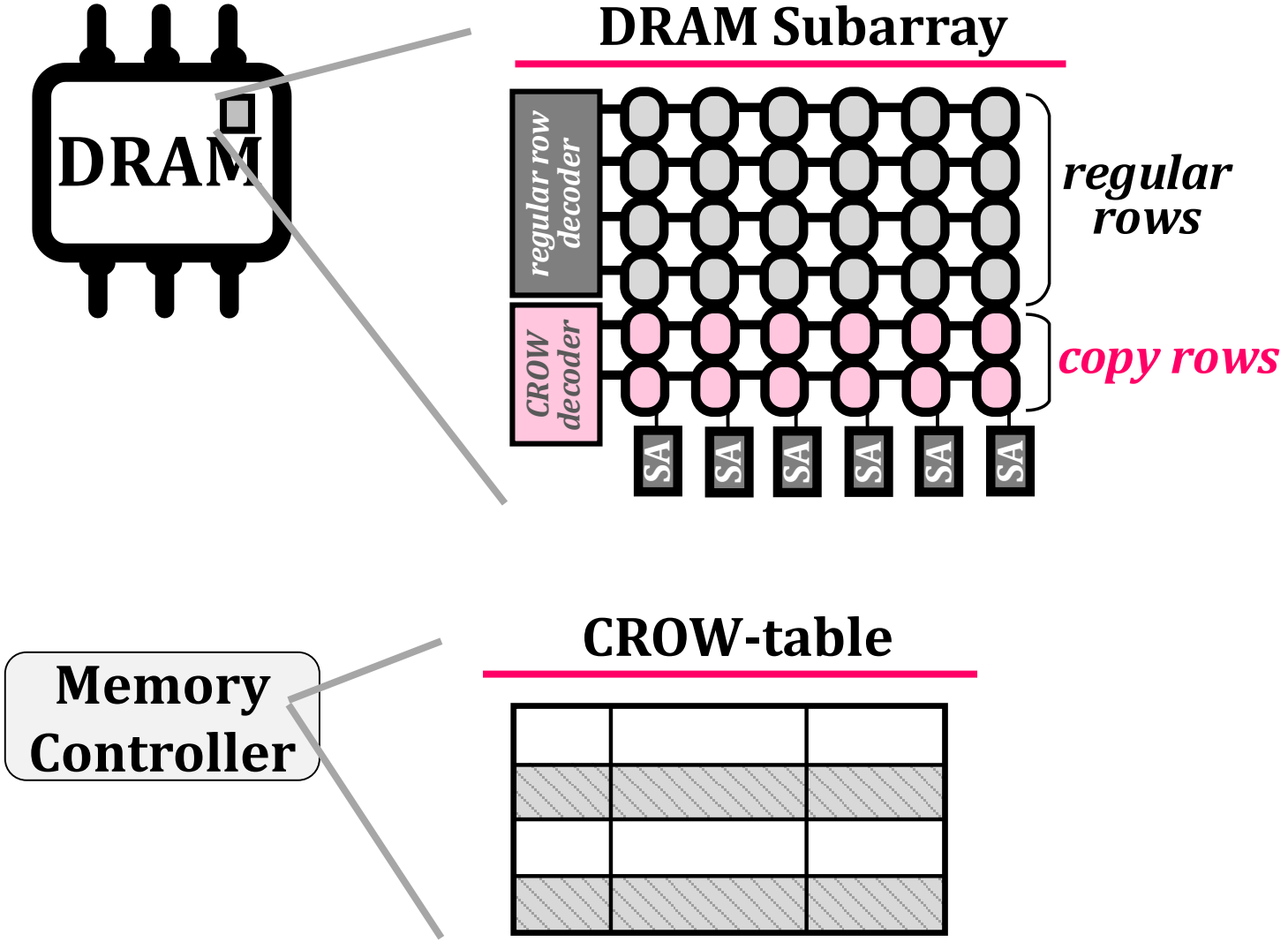
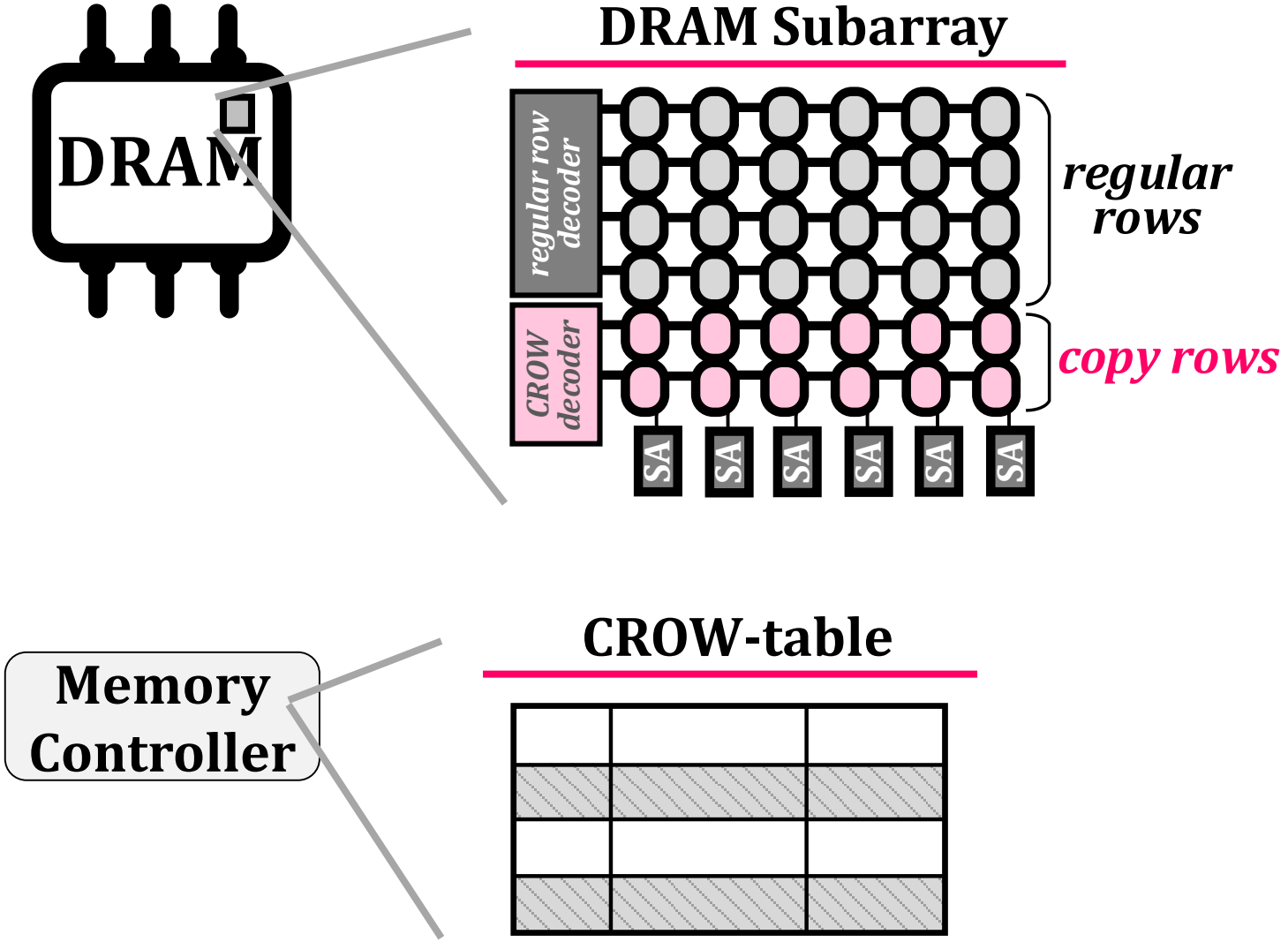


Request Queue

`load row X`

CROW-cache Operation

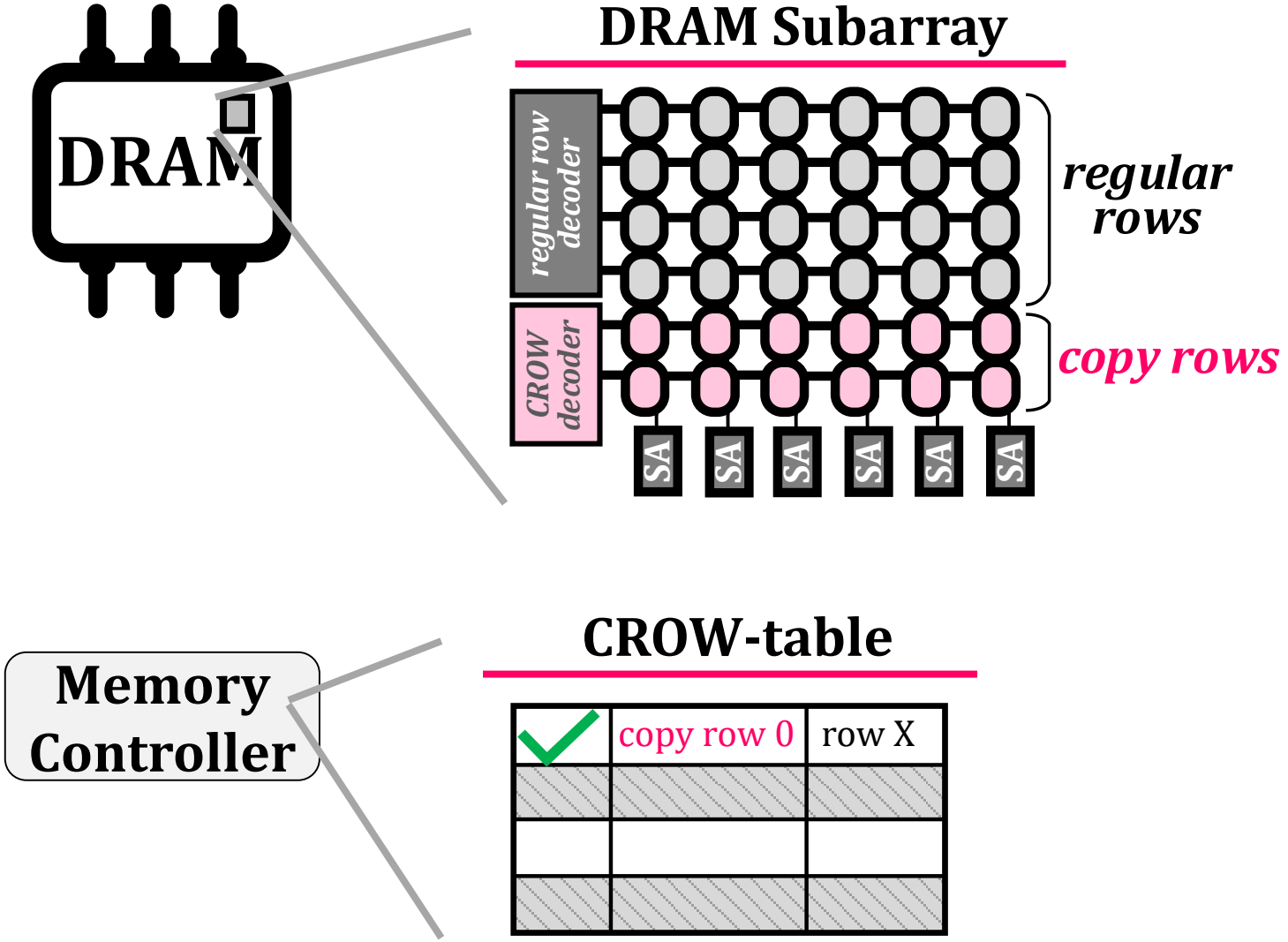


Request Queue

`load row X`

1 CROW-table miss

CROW-cache Operation



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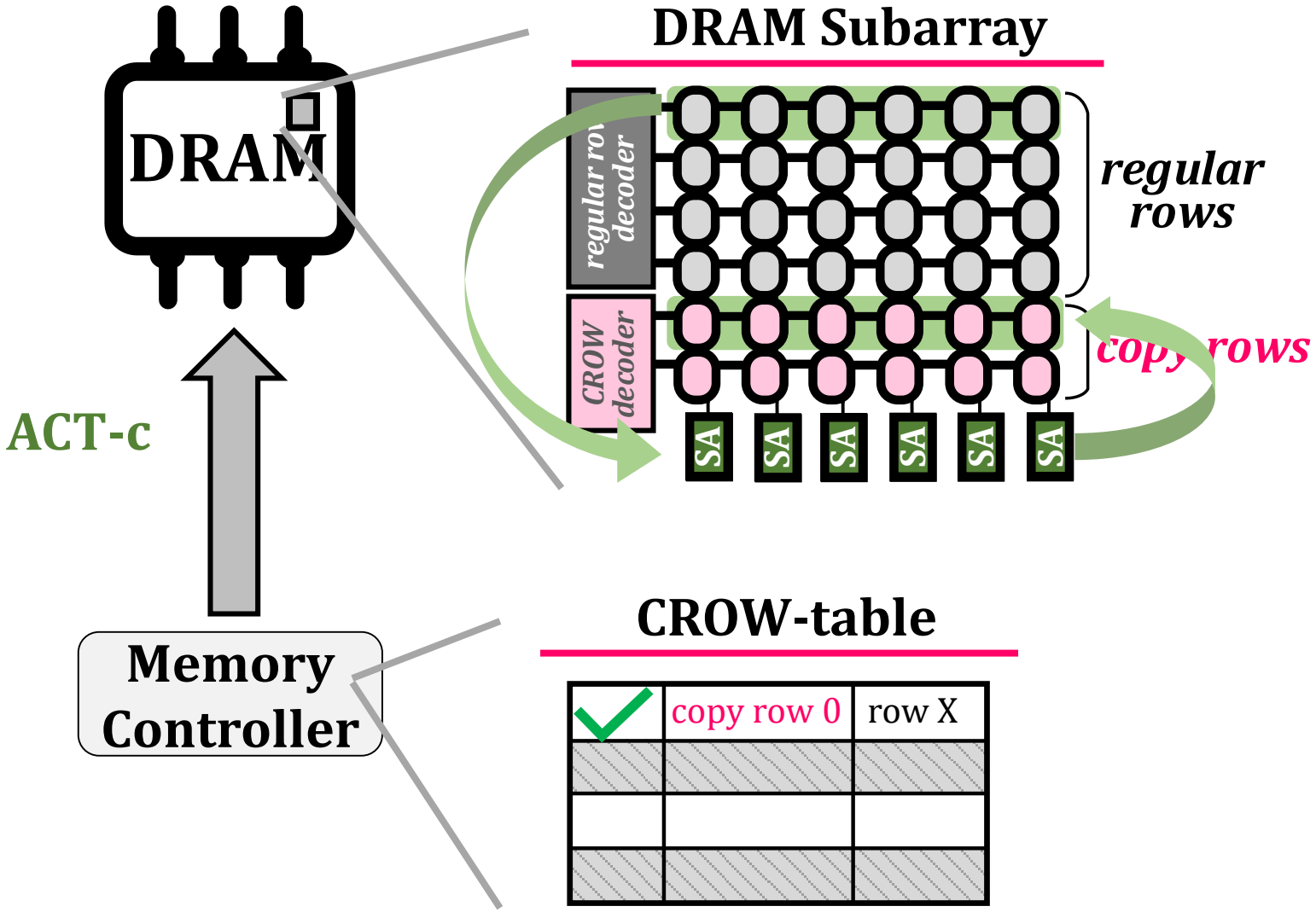
`load row X`

1. CROW-table miss
2. Allocate a copy row

CROW-cache Operation

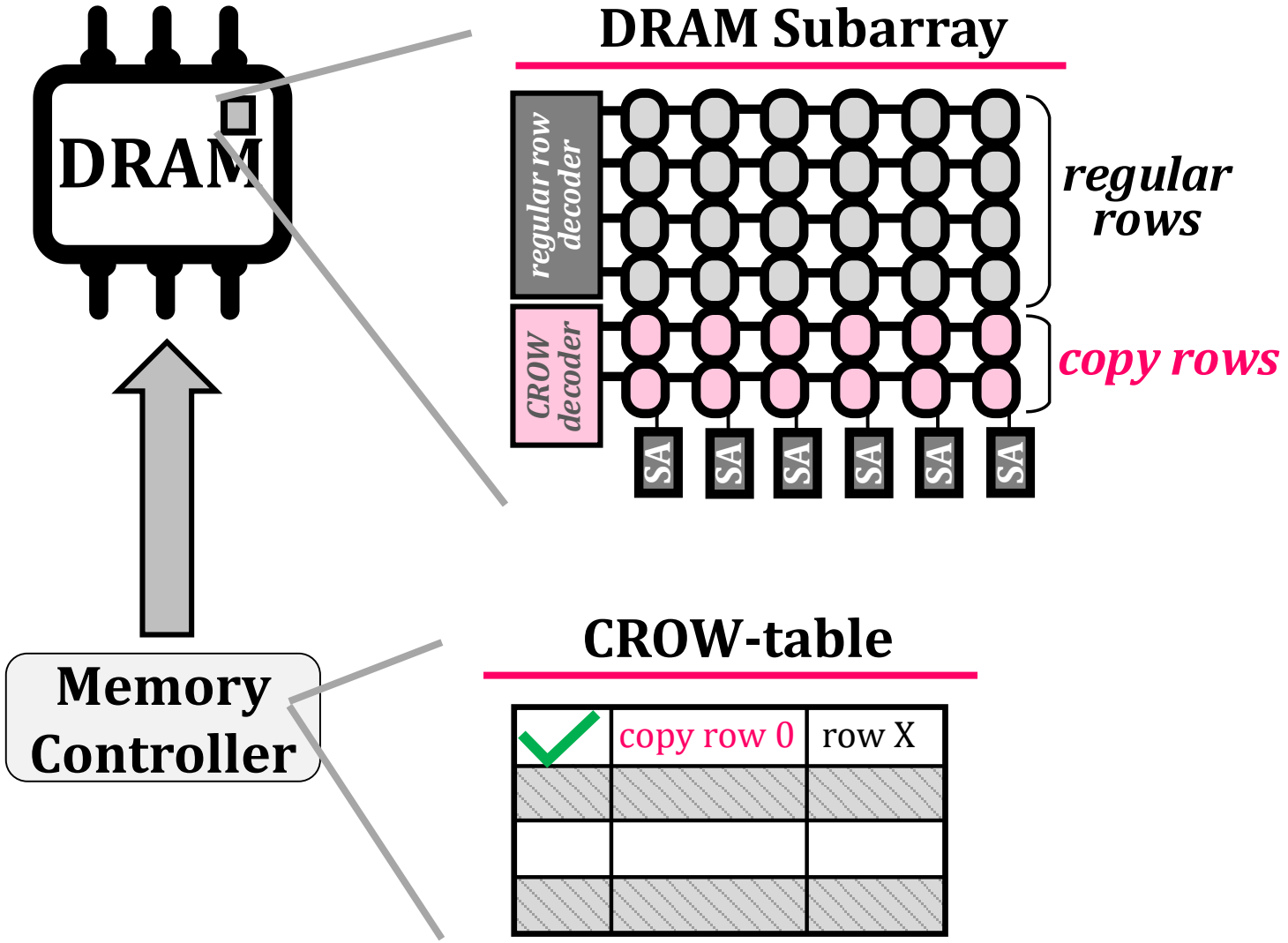


Request Queue

`load row X`

1. CROW-table miss
2. Allocate a copy row
3. Issue ACT-c (copy)

CROW-cache Operation



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`load row X`

`[bank conflict]`

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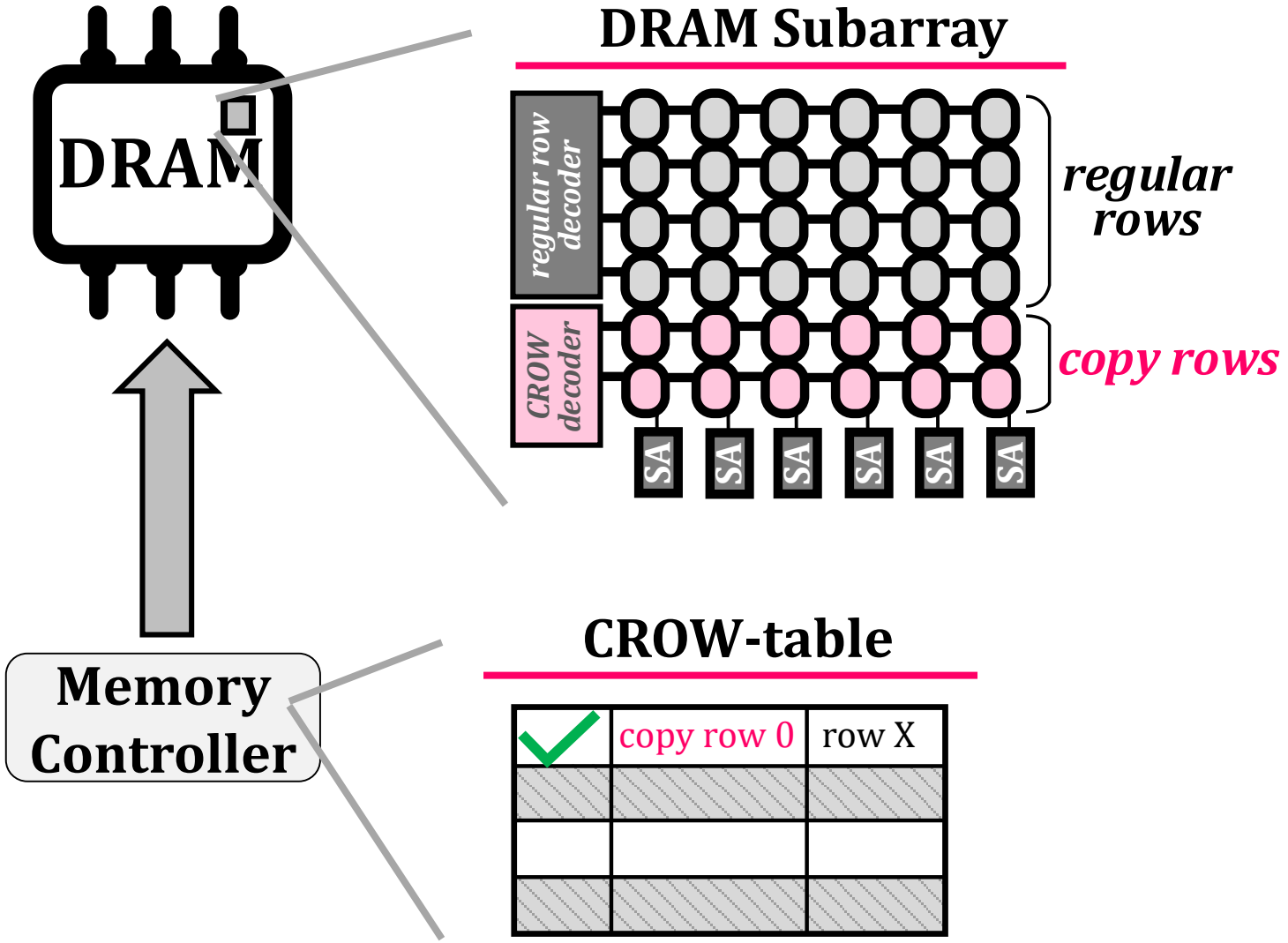

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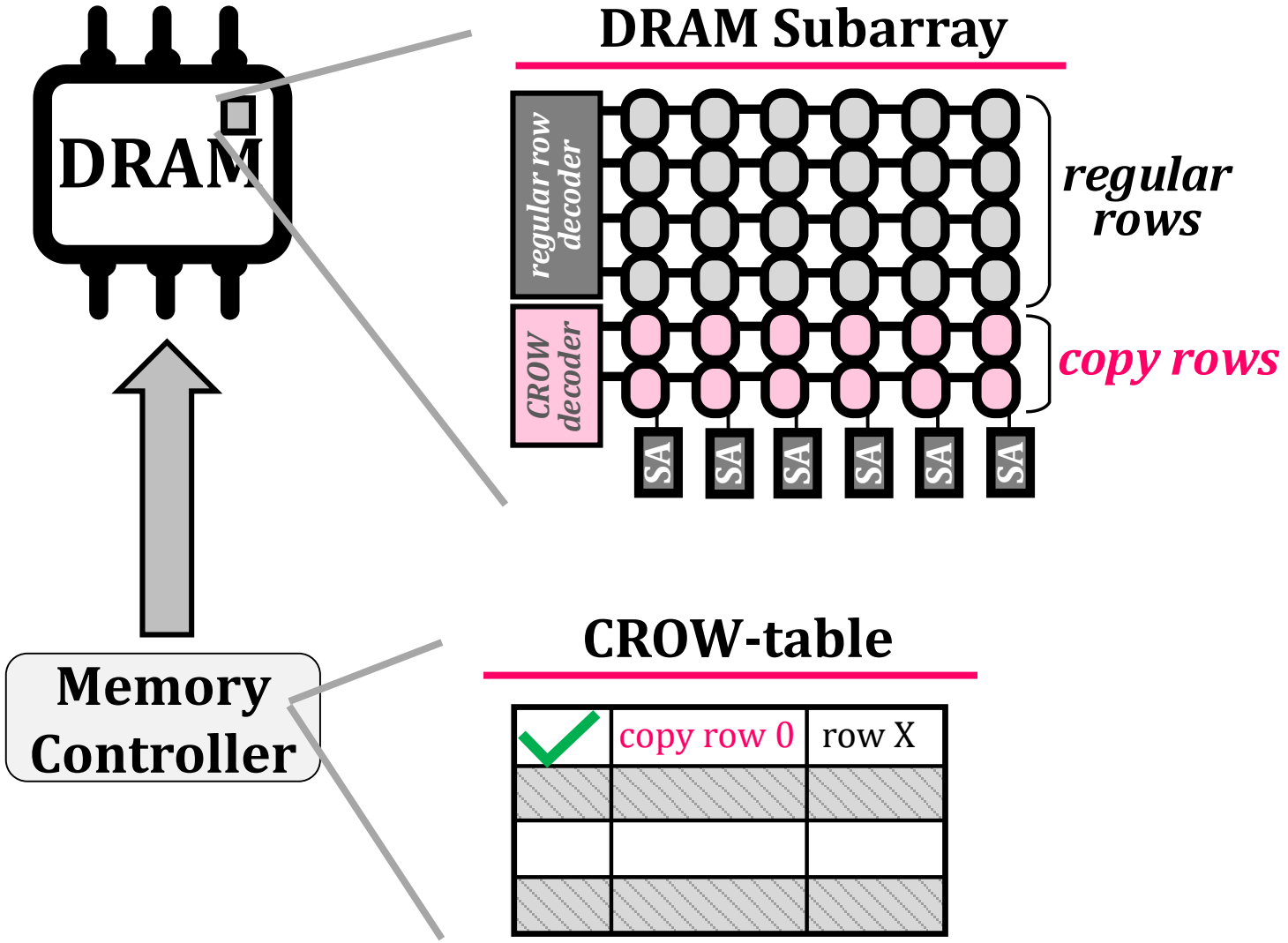

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`load row X`

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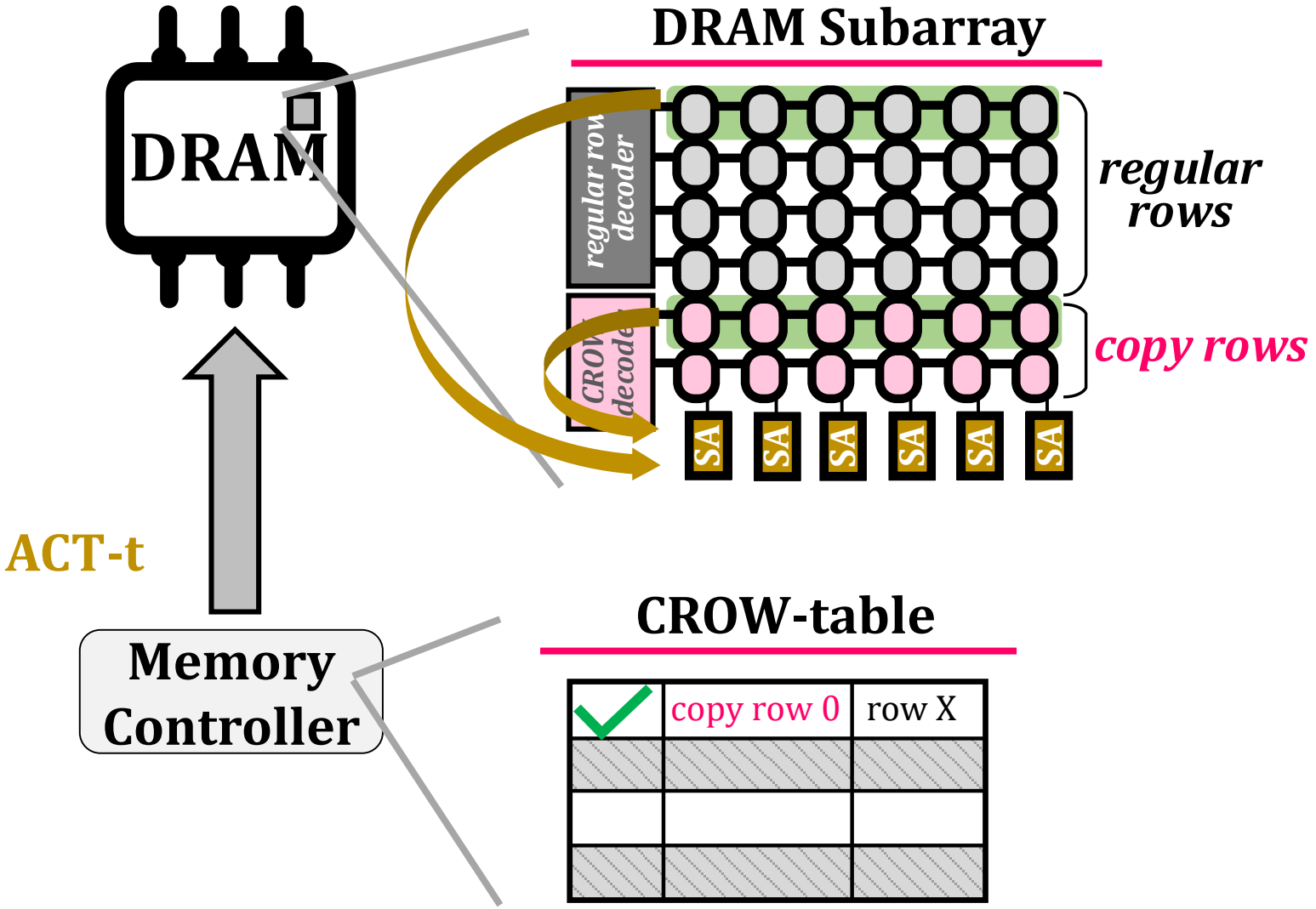
`load row X`

1. CROW-table miss
2. Allocate a copy row
3. Issue ACT-c (copy)
1. CROW-table hit

CROW-cache Operation



Request Queue

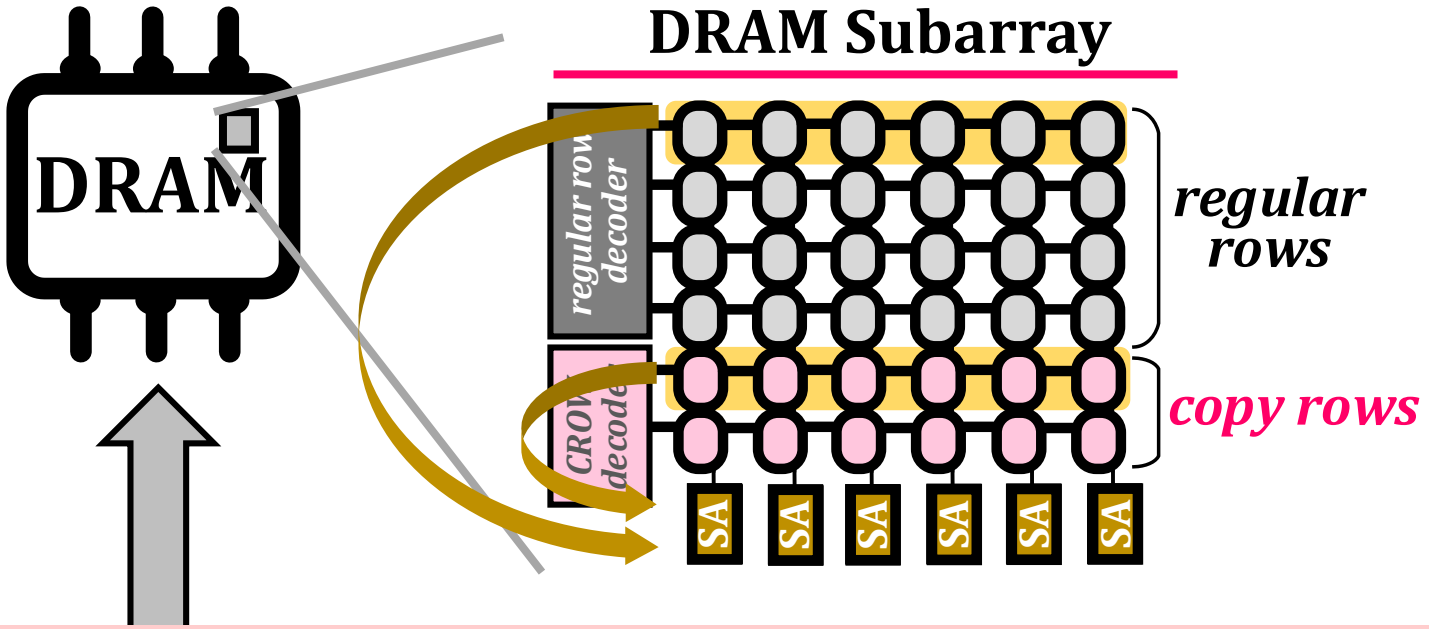
`load row X`

`[bank conflict]`

`load row X`

1. CROW-table miss
2. Allocate a copy row
3. Issue ACT-c (copy)
1. CROW-table hit
2. Issue ACT-t (two row)

CROW-cache Operation



Request Queue

```
load row X
[bank conflict]
load row X
```

1. CROW-table miss
2. Allocate a copy row

Second activation of row X is faster

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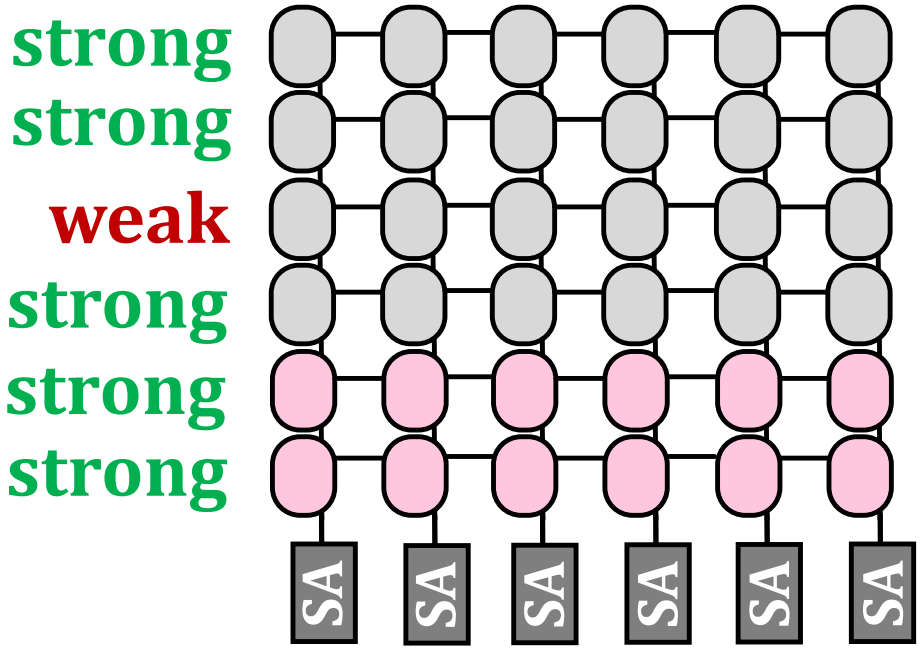
CROW-ref **eliminates more than half of the refresh** requests

CROW-ref Operation

CROW-ref Operation

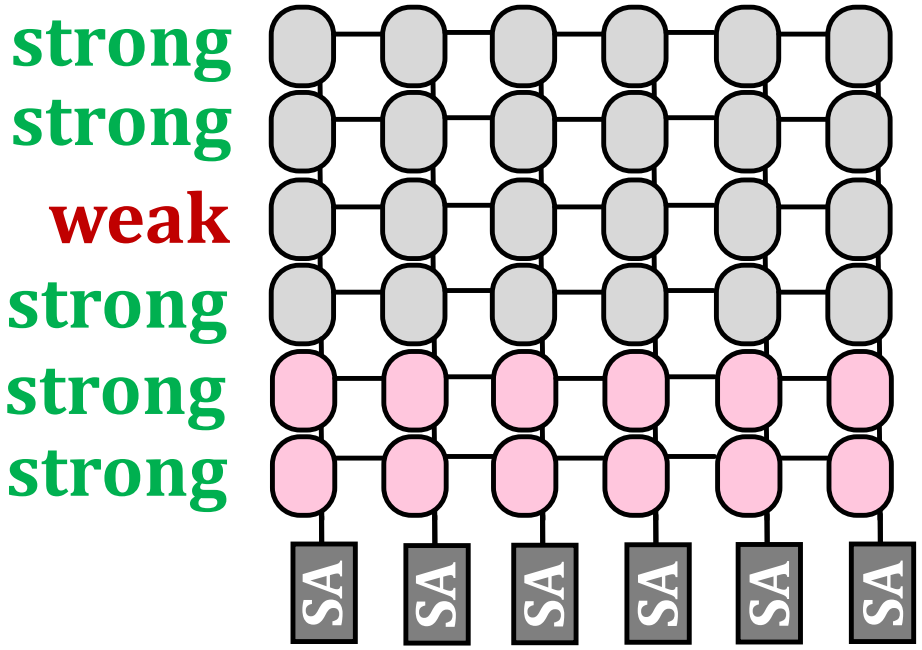
Retention Time Profiler



❶ Perform retention time profiling

CROW-ref Operation

Retention Time Profiler



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CROW-ref Operation

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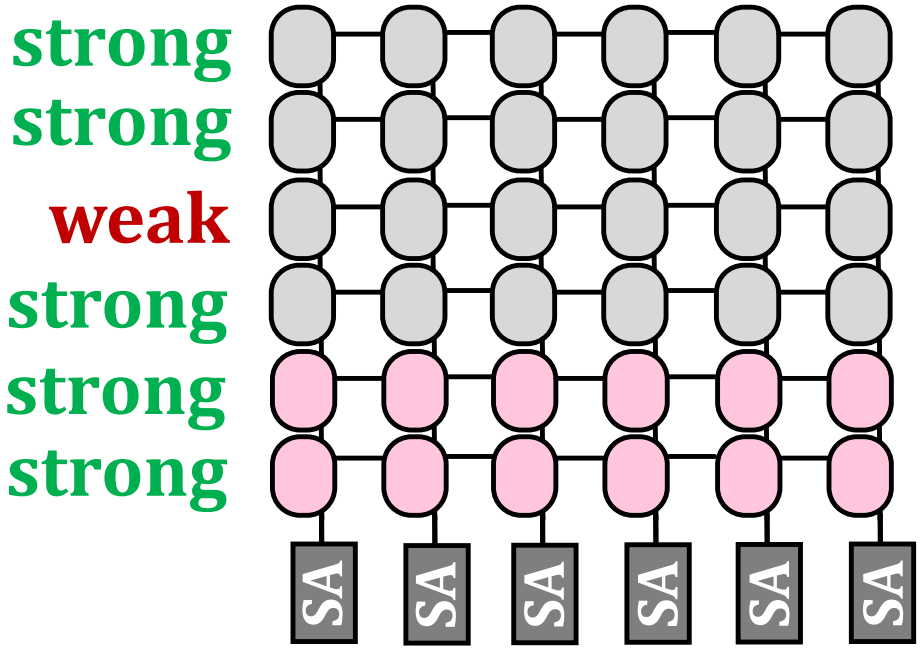

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CROW-ref Operation

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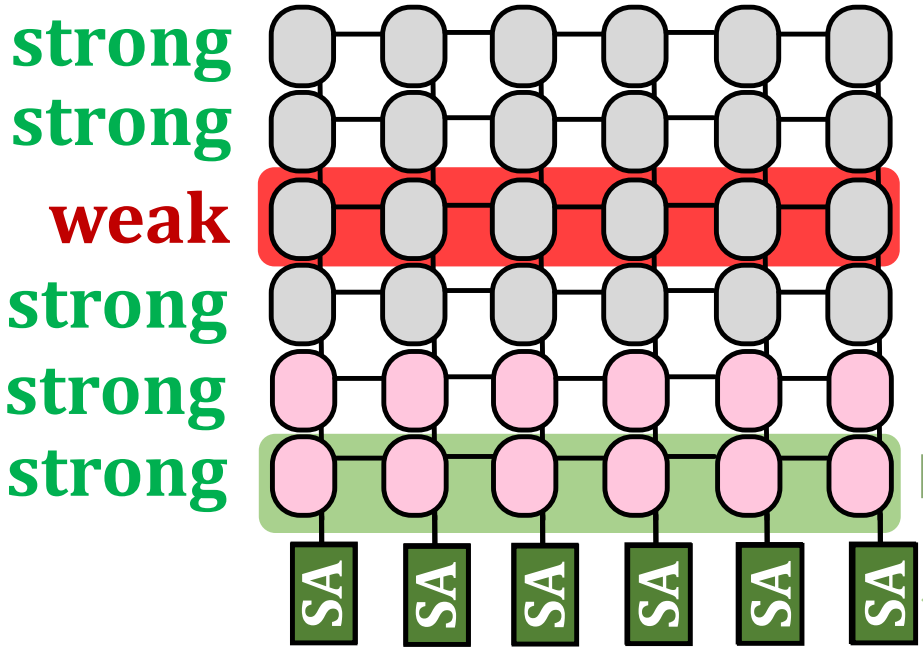

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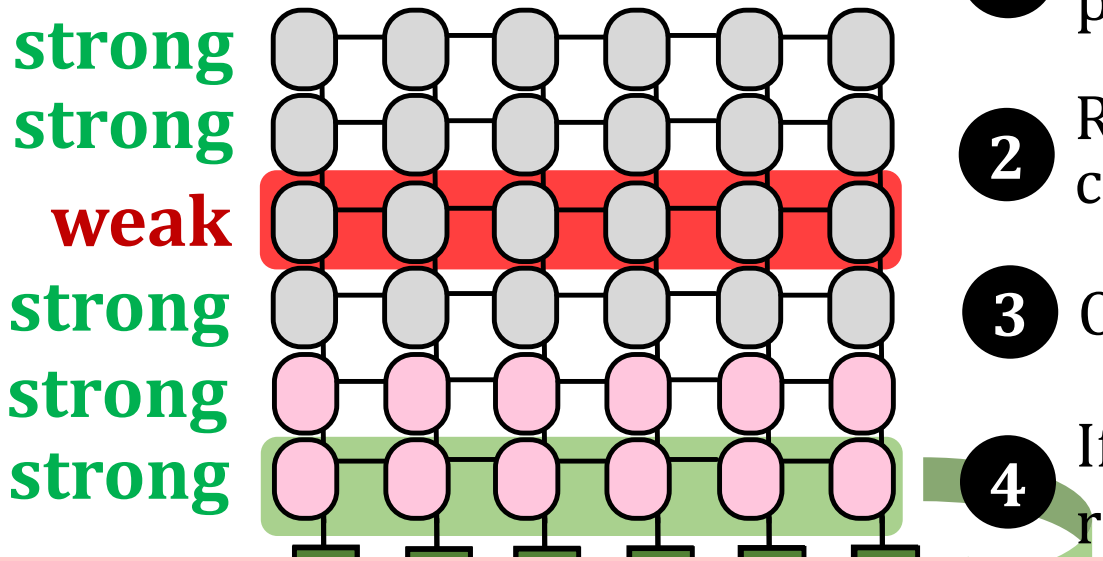
CROW-ref Operation

Retention Time



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How many weak rows exist in a DRAM chip?

Identifying Weak Rows

Weak cells are rare *[Liu+, ISCA'13]*

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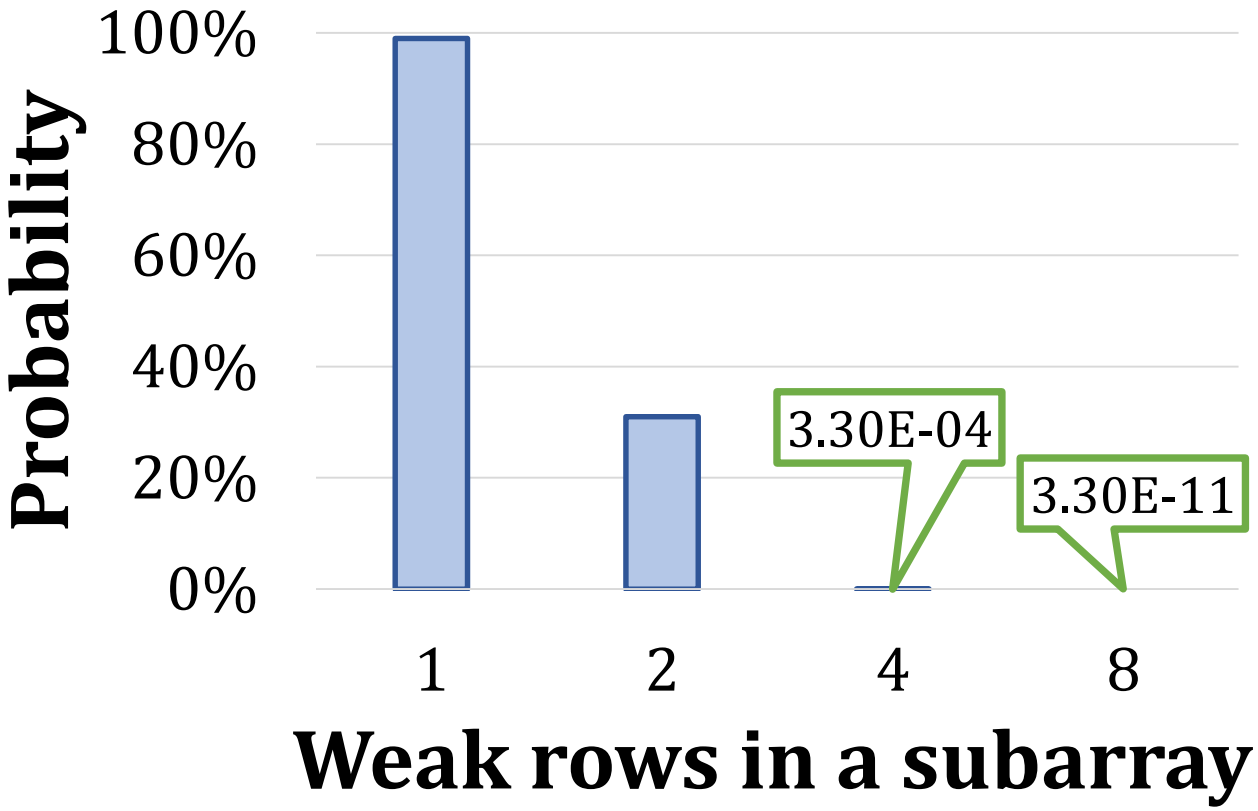

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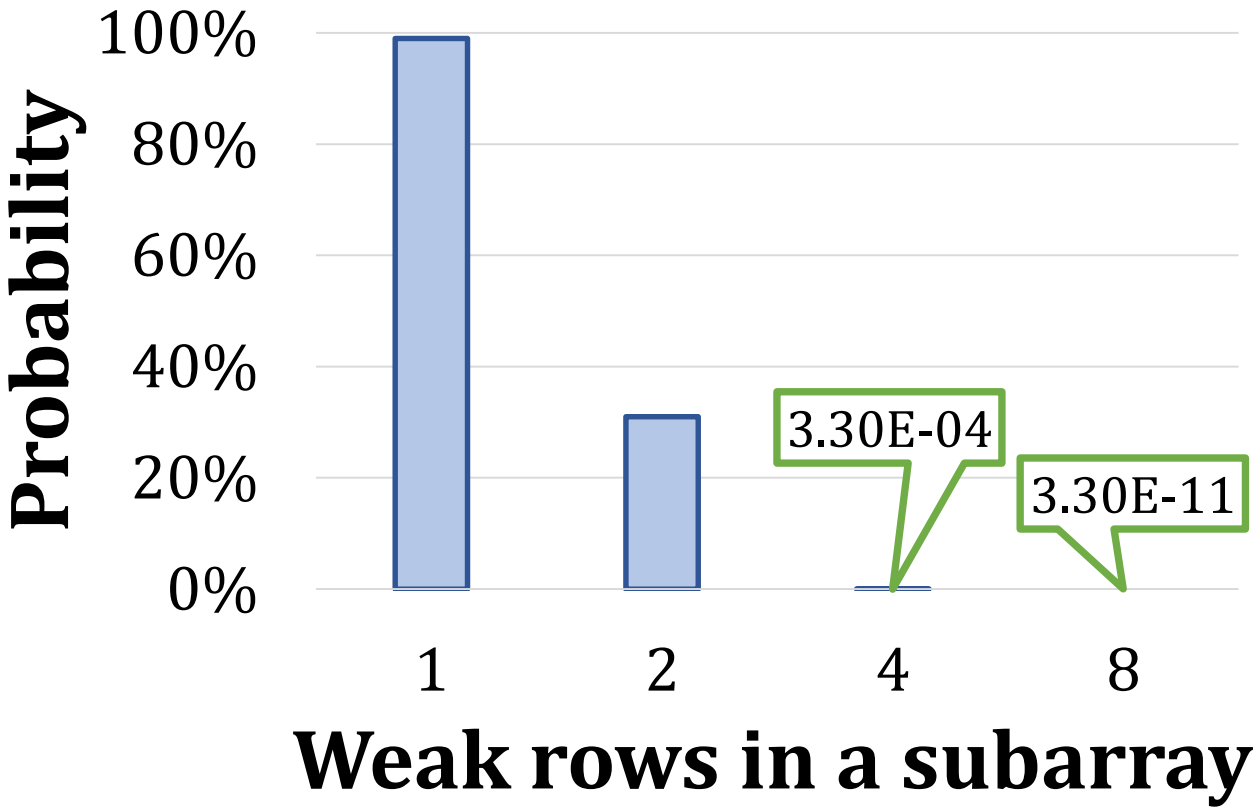

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DRAM Retention Time Profiler

- REAPER *[Patel+, ISCA'17]*
  PARBOR *[Khan+, DSN'16]*
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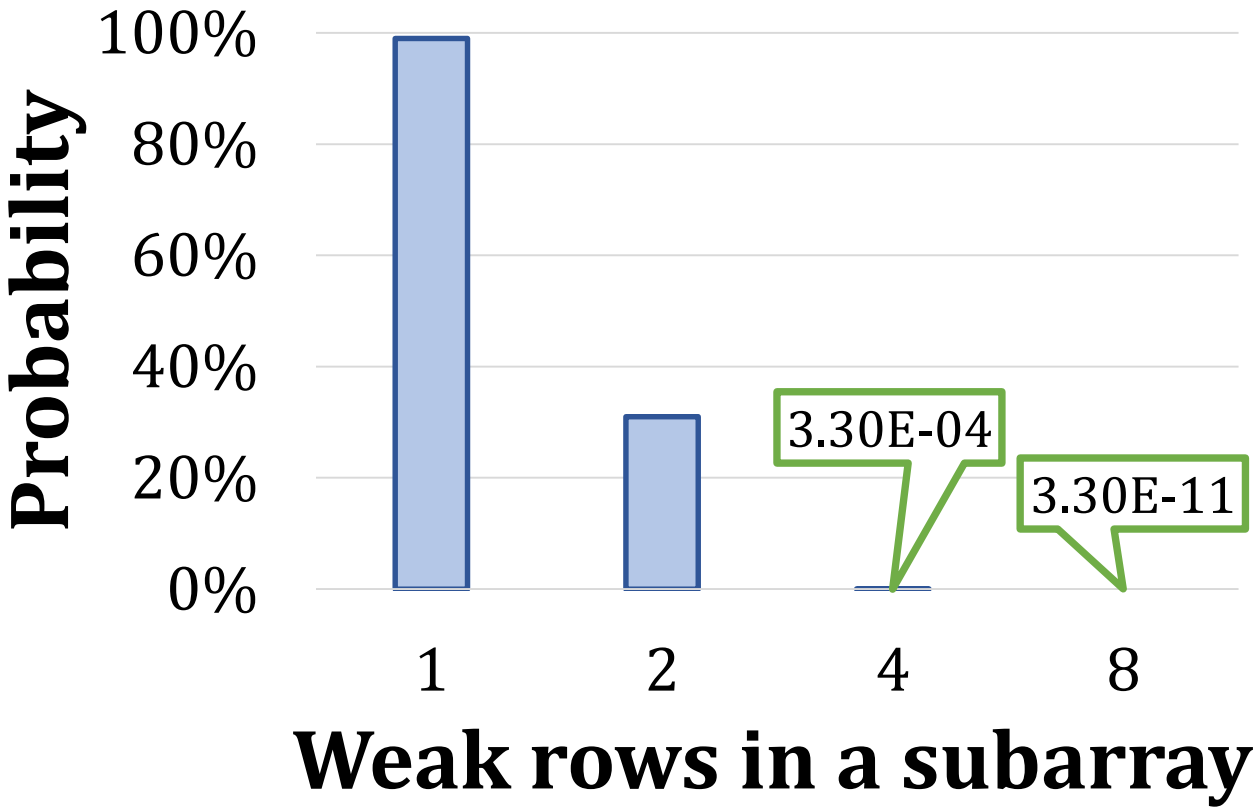

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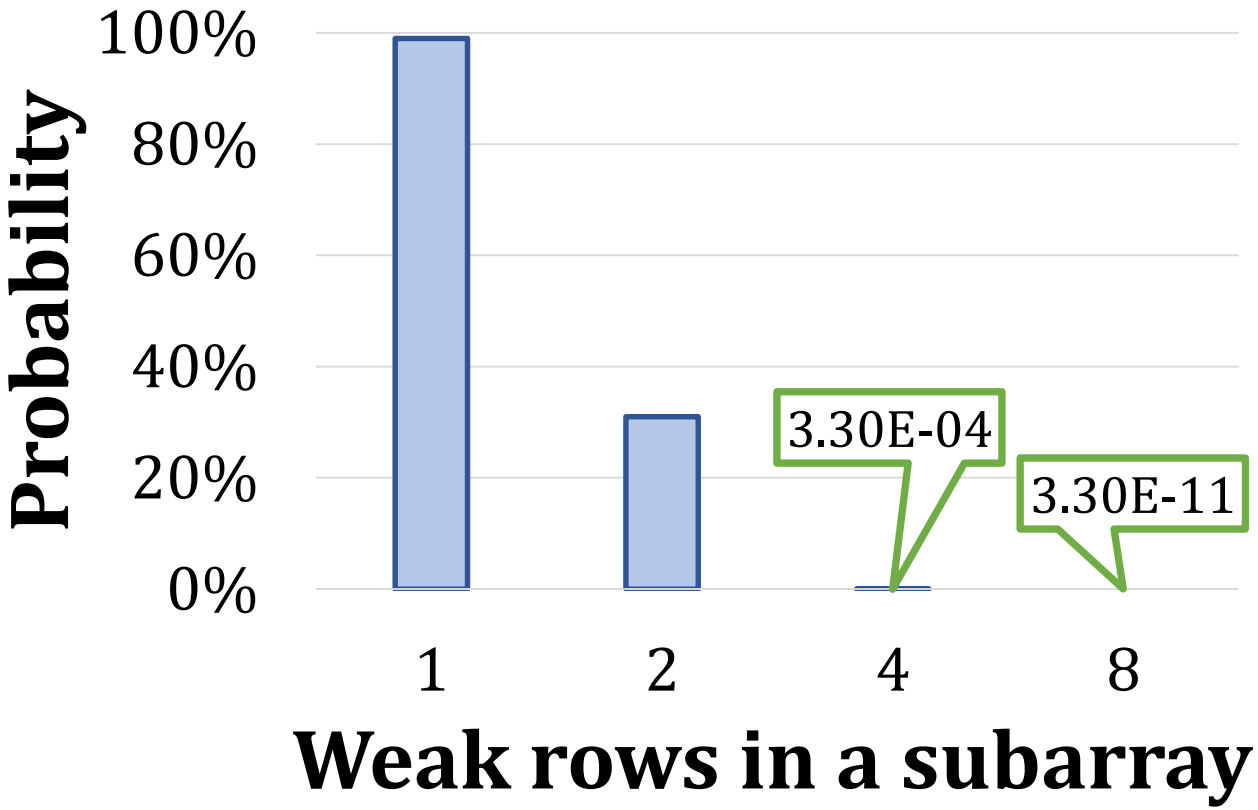
DRAM Retention Time Profiler

- REAPER *[Patel+, ISCA'17]*
  PARBOR *[Khan+, DSN'16]*
  AVATAR *[Qureshi+, DSN'15]*
- At system *boot* or during *runtime*



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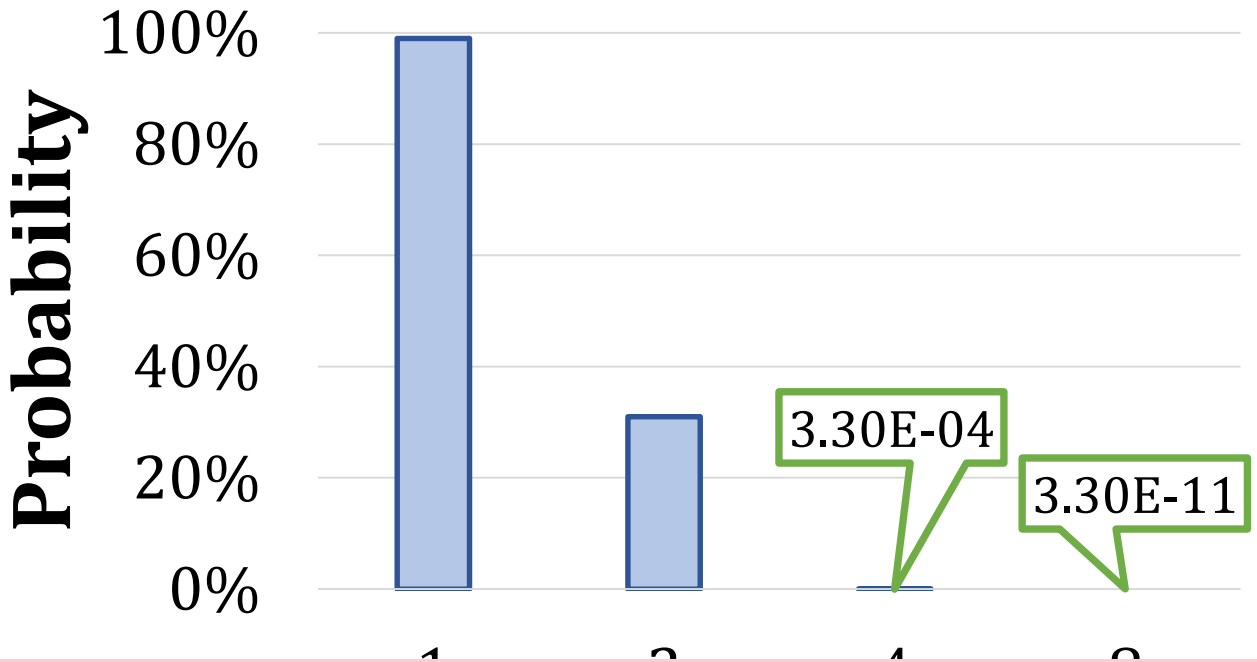

A few copy rows are sufficient to halve the refresh rate

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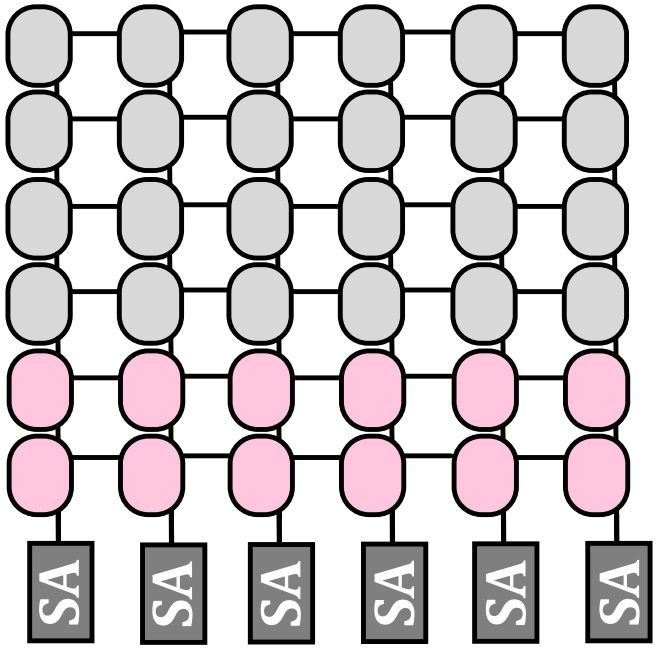

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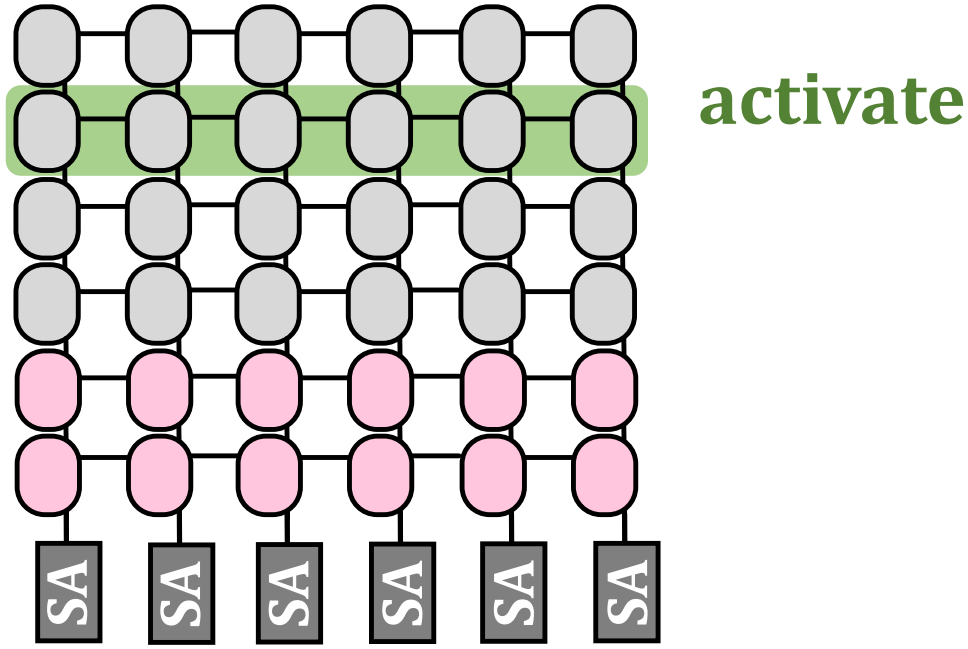

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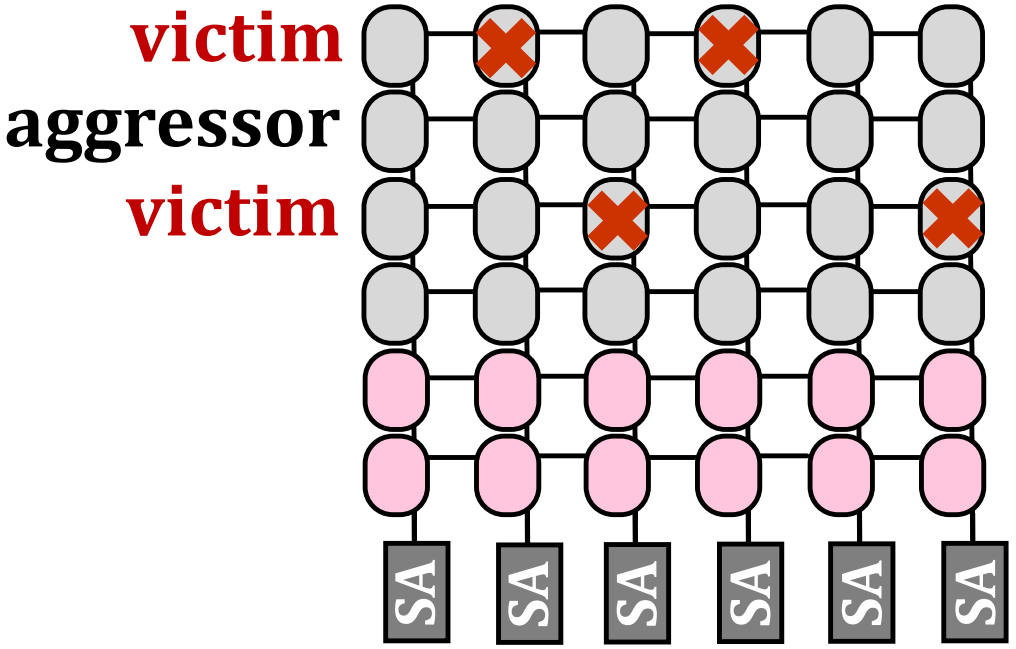

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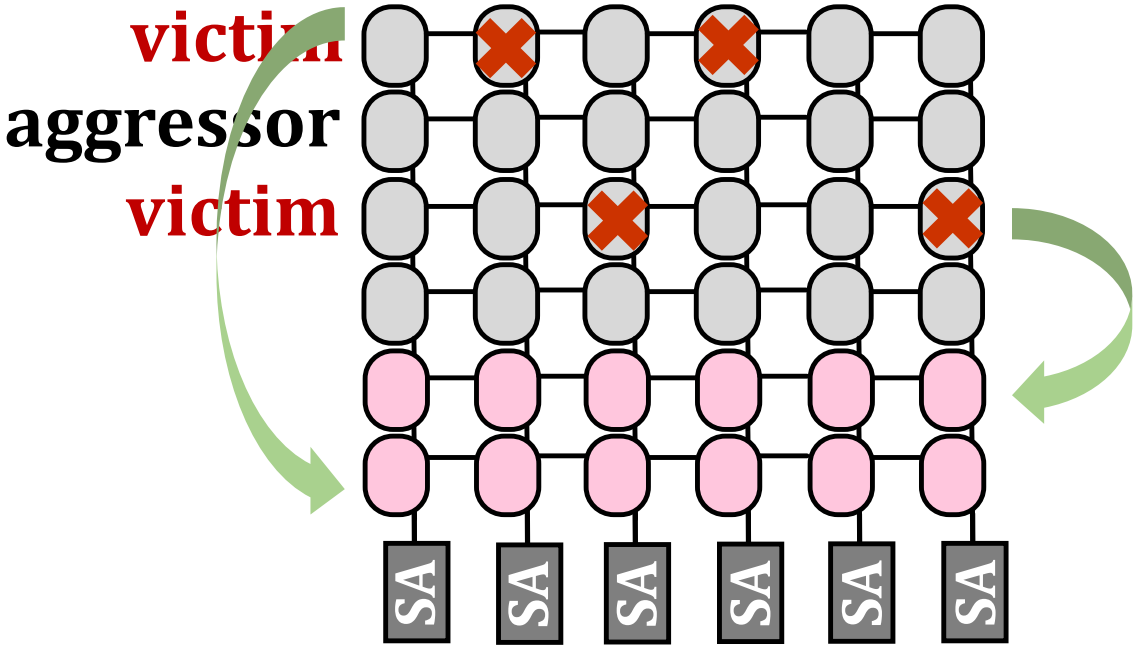

Key idea: remap victim rows to copy rows

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Methodology

- **Simulator**
  - DRAM Simulator (Ramulator *[Kim+, CAL'15]*)
    https://github.com/CMU-SAFARI/ramulator

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- **Workloads**
  - 44 single-core workloads
    - *SPEC CPU2006, TPC, STREAM, MediaBench*
  - 160 multi-programmed four-core workloads
    - *By randomly choosing from single-core workloads*
  - Execute at least 200 million representative instructions per core

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- **System Parameters**
  - 1/4 core system with 8 MiB LLC
  - LPDDR4 main memory
  - 8 copy rows per 512-row subarray

CROW-cache Results

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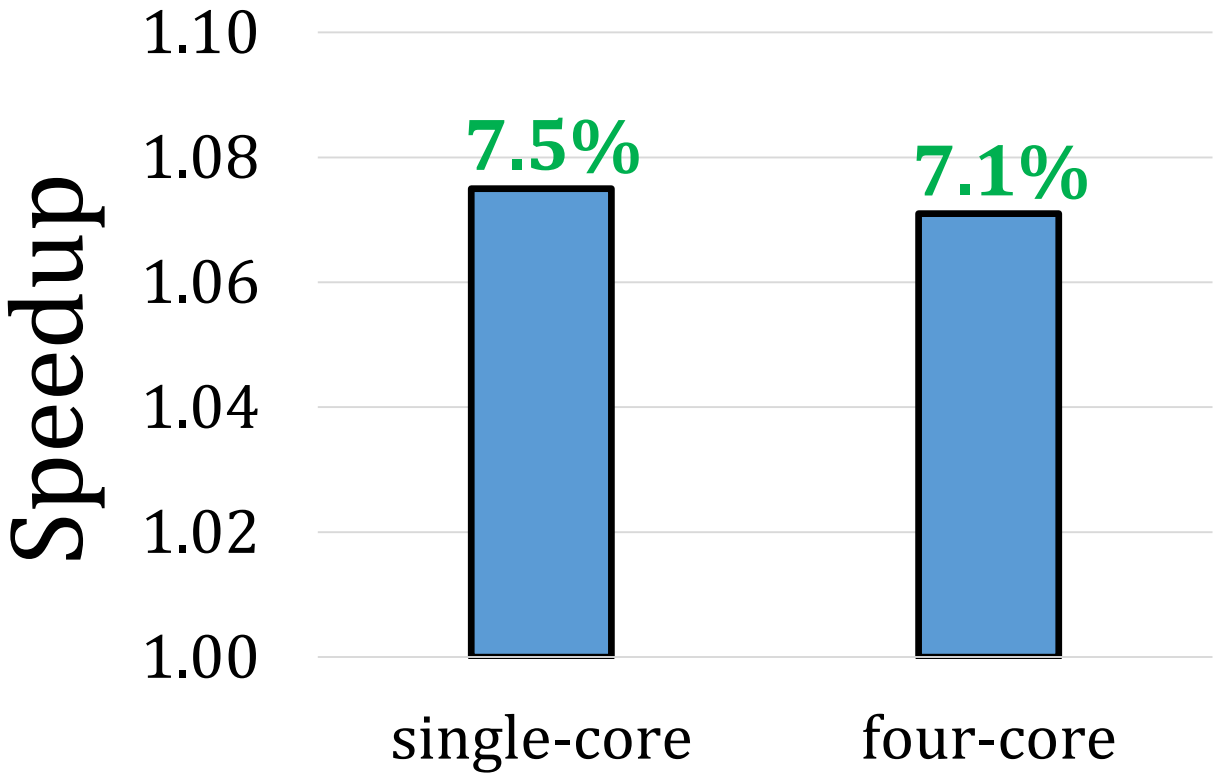

** with 8 copy rows and a 64Gb DRAM chip (sensitivity in paper)*

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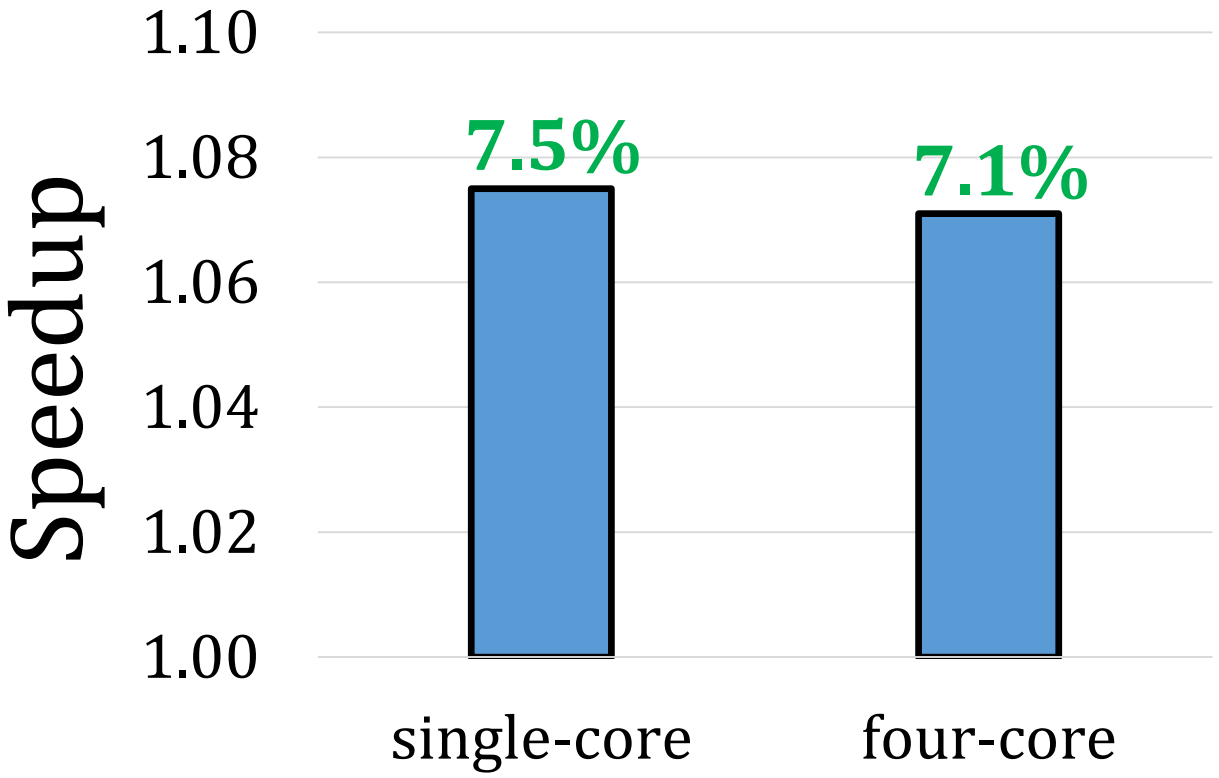

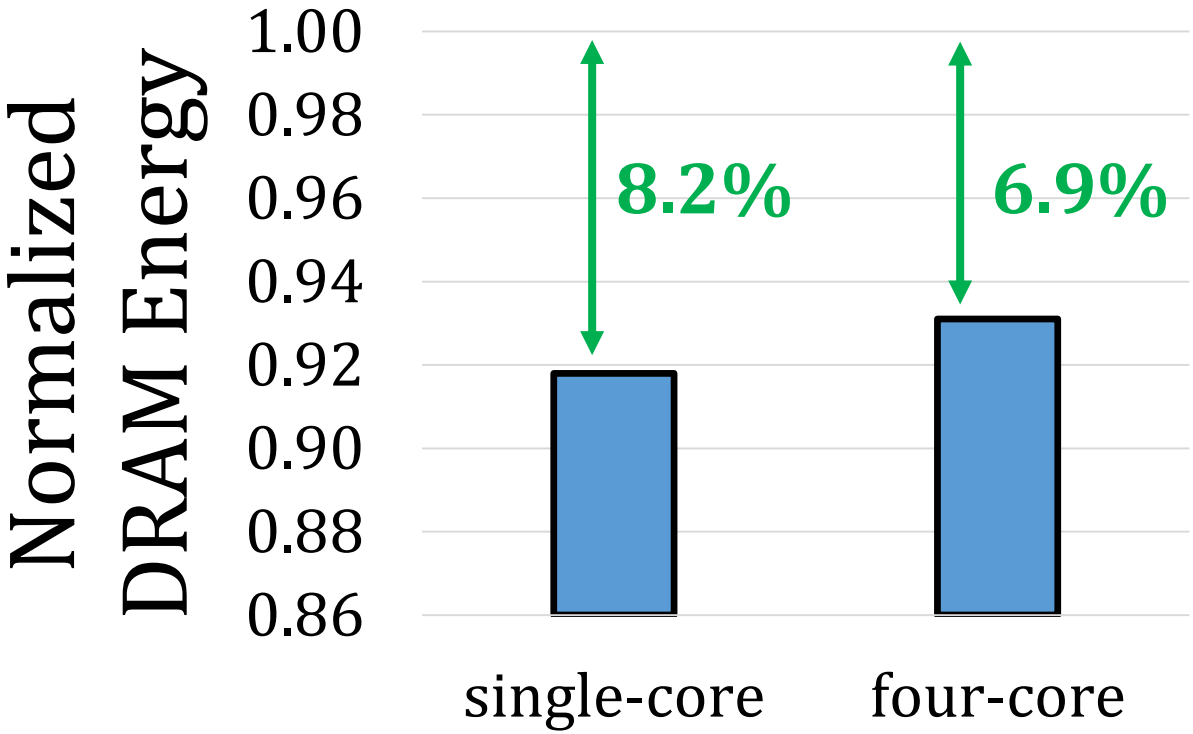

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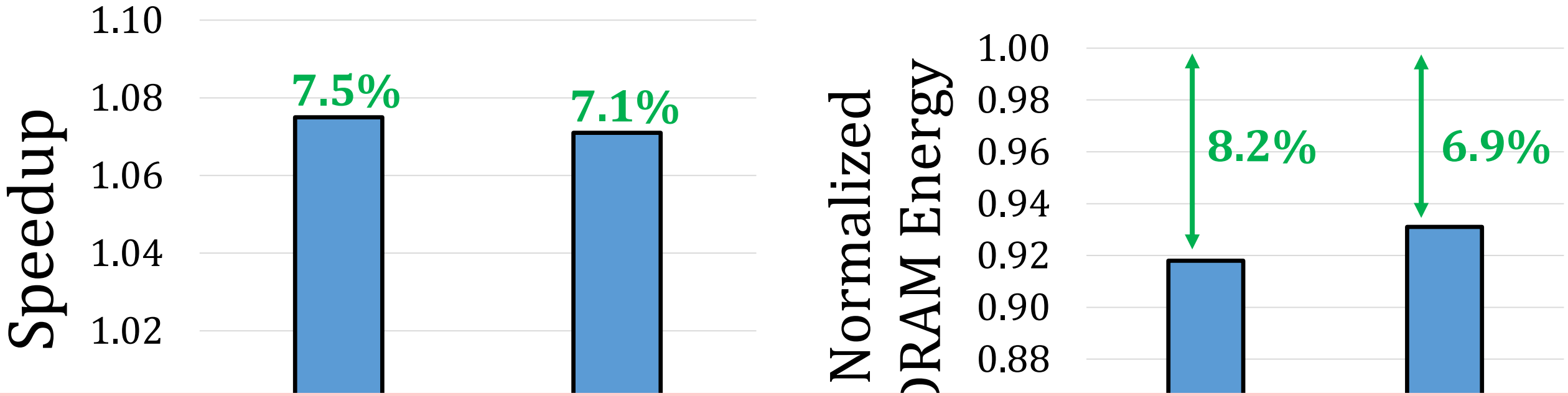

CROW-cache **improves** single-/four-core **performance** and **energy**

CROW-ref Results

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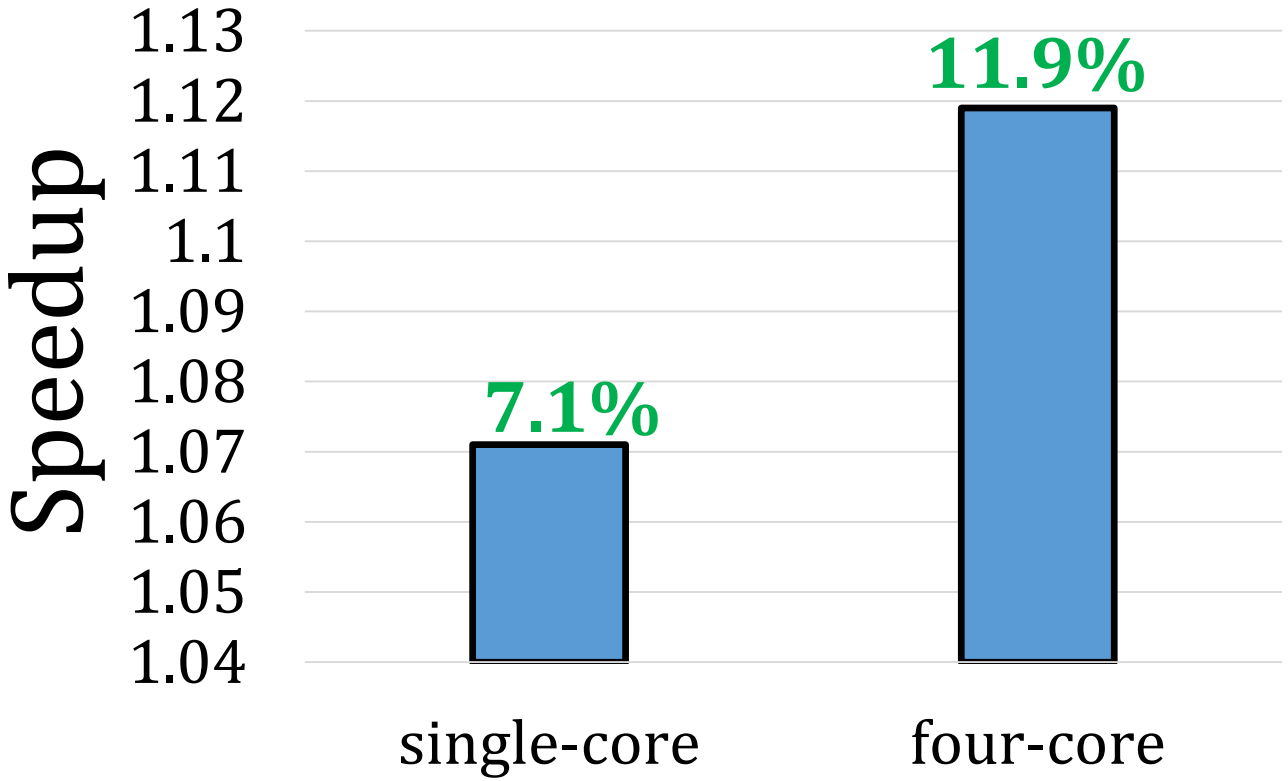

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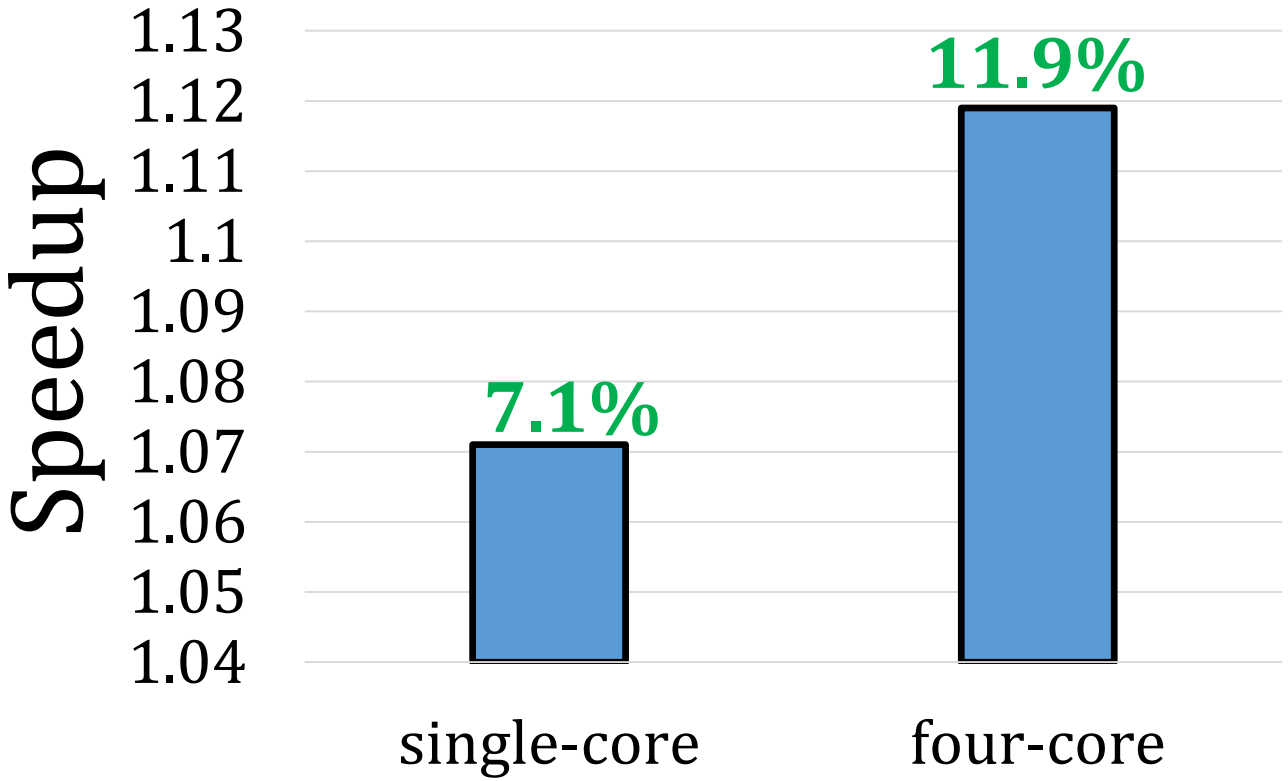

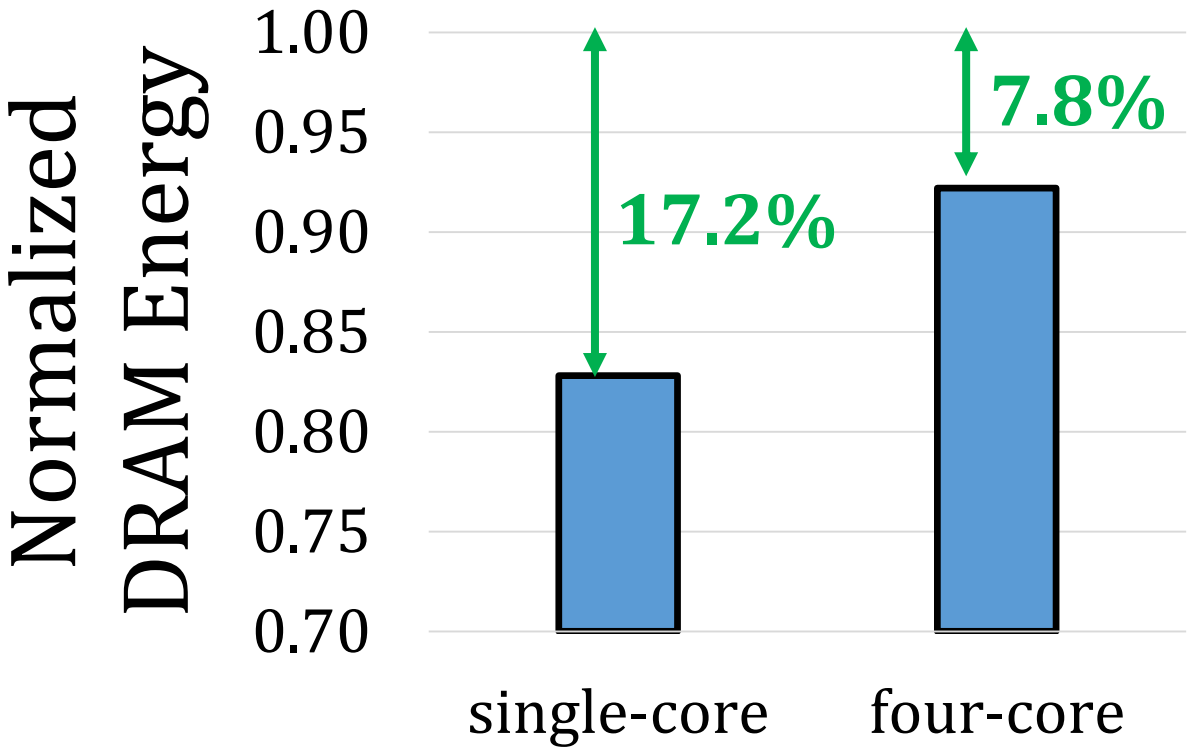

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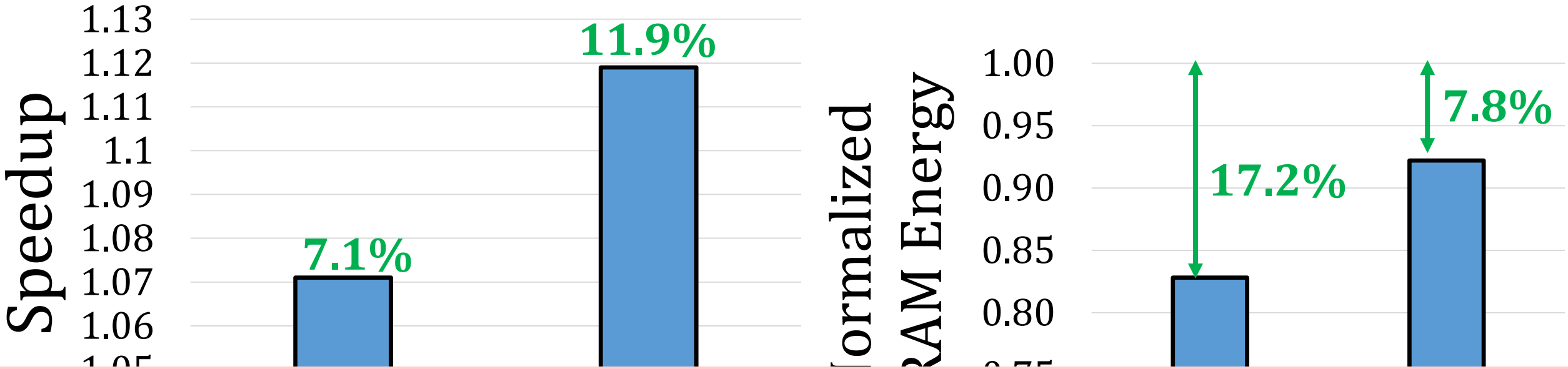
CROW-ref Results



CROW-ref significantly reduces the performance and energy overhead of DRAM refresh

Combining CROW-cache and CROW-ref

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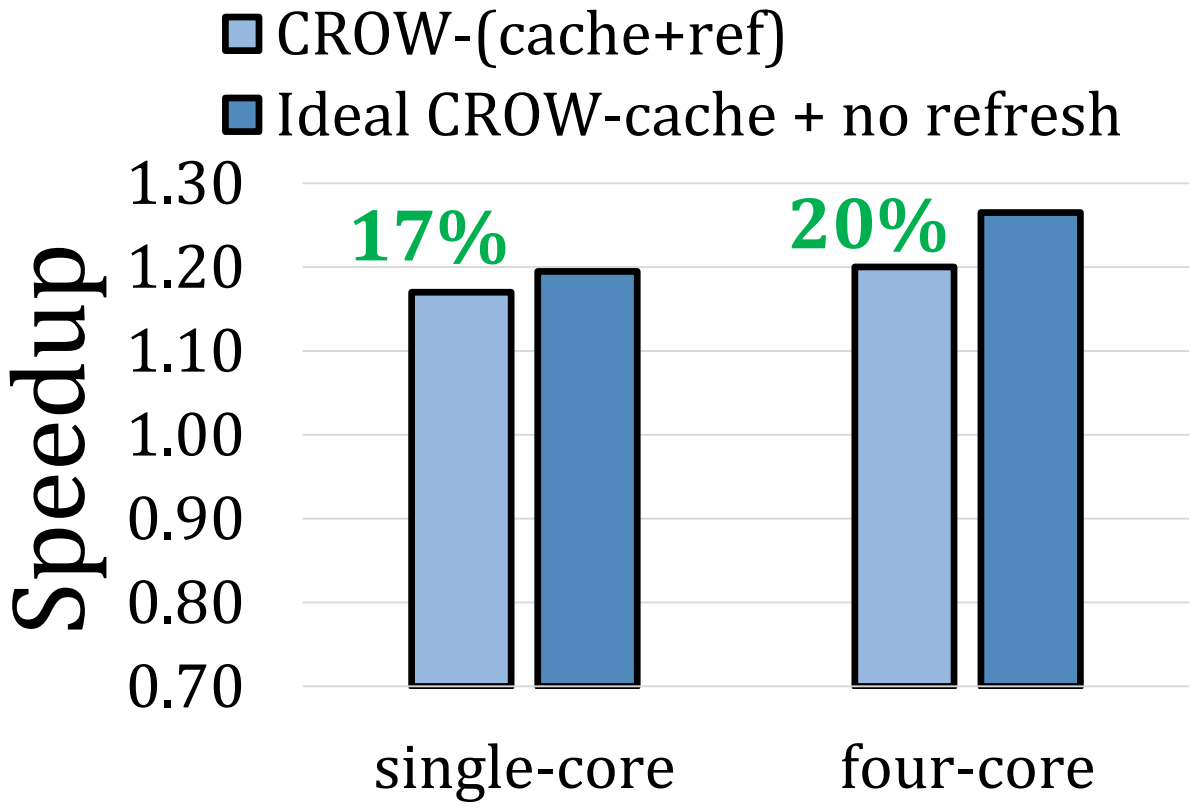

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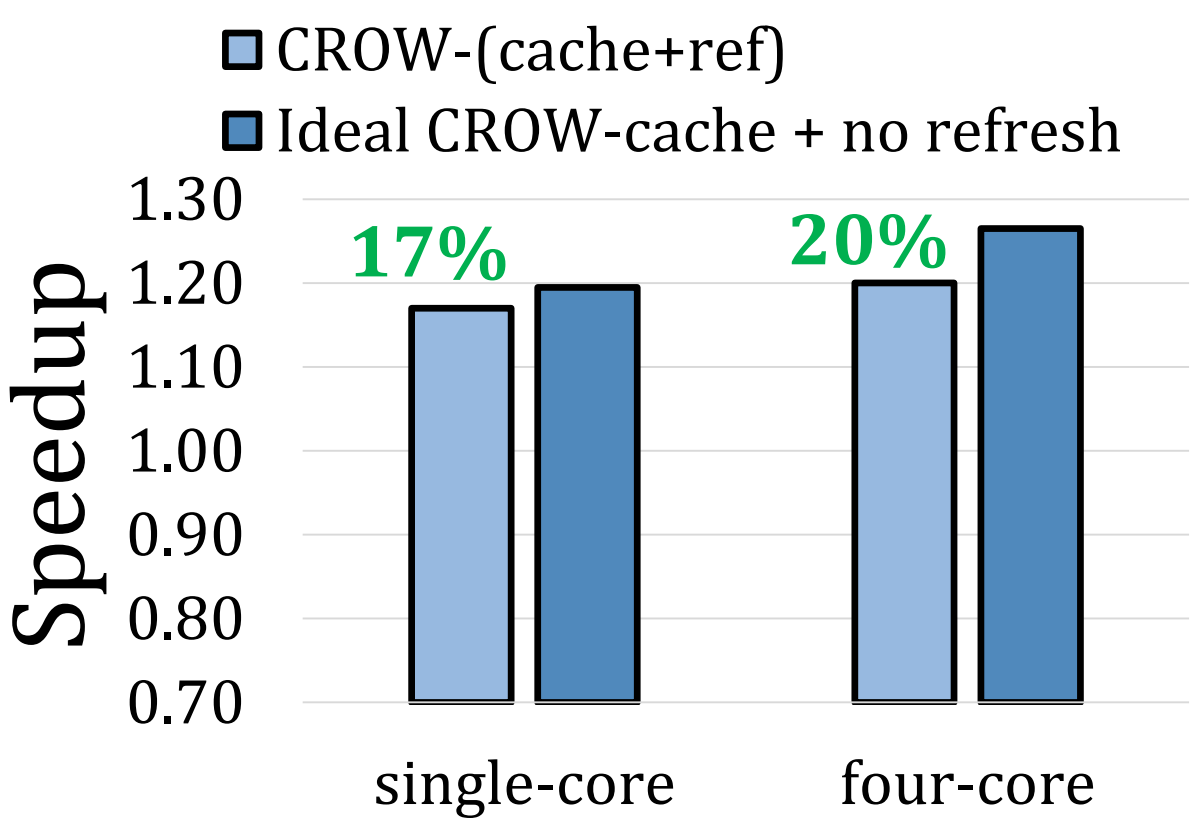

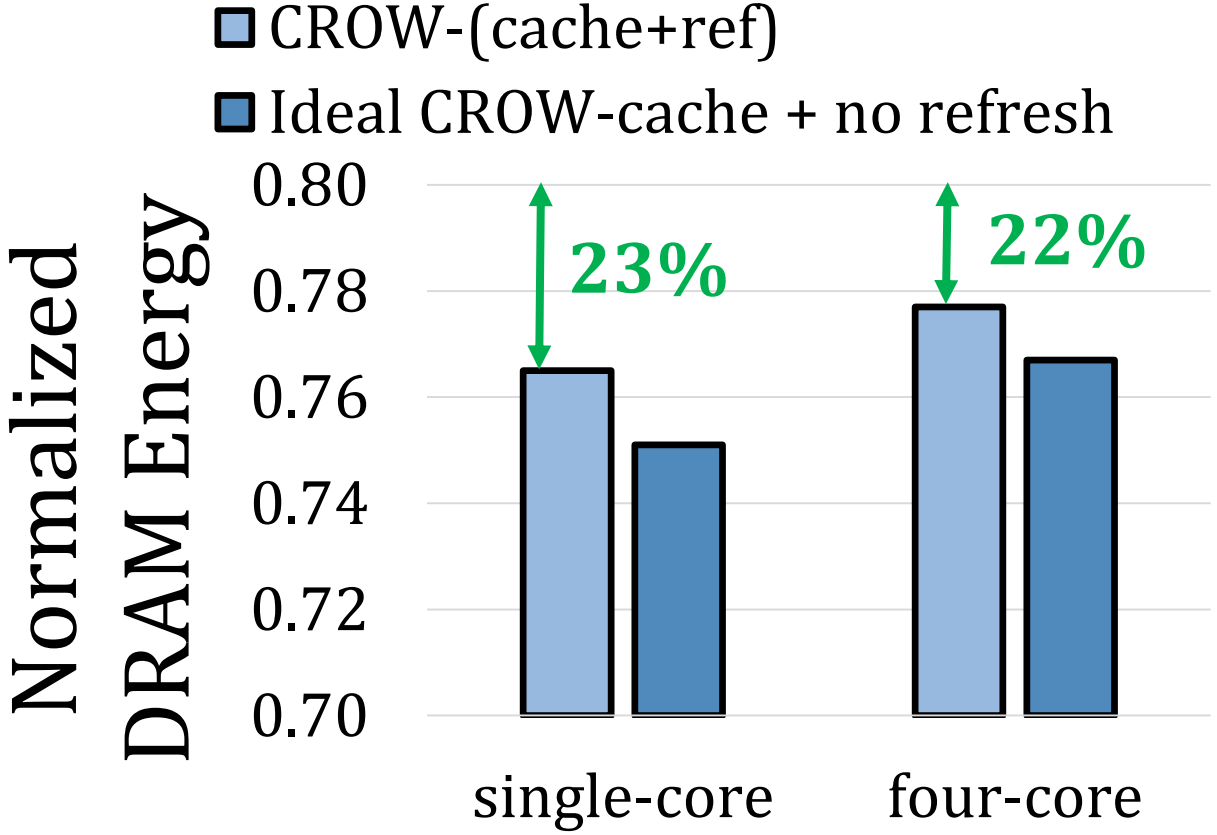

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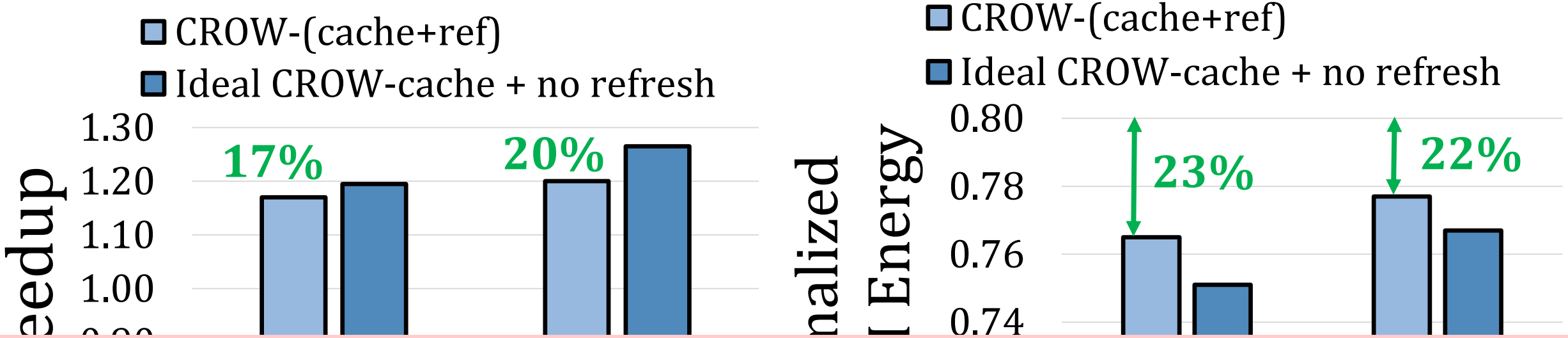

CROW-(cache+ref) provides more performance and DRAM energy benefits than each mechanism alone

Hardware Overhead

For 8 copy rows and 16 GiB DRAM:

- 0.5% DRAM chip area
- 1.6% DRAM capacity
- 11.3 KiB memory controller storage

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CROW is a low-cost substrate

Other Results in the Paper

Other Results in the Paper

- Performance and energy sensitivity to:
  - Number of copy-rows per subarray
  - DRAM chip density
  - Last-level cache capacity

- CROW-cache with prefetching

- CROW-cache compared to other in-DRAM caching mechanisms:
  - TL-DRAM *[Lee+, HPCA'13]*
  - SALP *[Kim+, ISCA'12]*

Outline

1. DRAM Operation Basics
2. The CROW Substrate
   - CROW-cache: Reducing DRAM Latency
   - CROW-ref: Reducing DRAM Refresh
   - Mitigating RowHammer
3. Evaluation
4. Conclusion

Conclusion

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github.com/CMU-SAFARI/CROW

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- **High access latency** → bottleneck for improving system performance/energy
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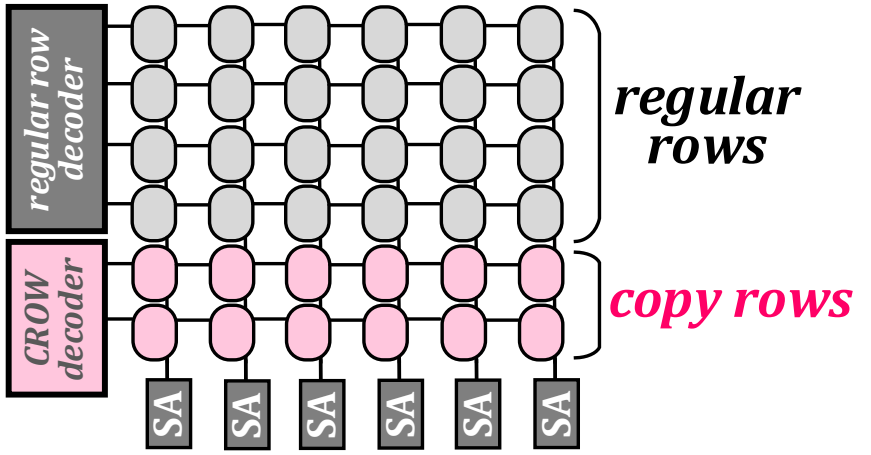

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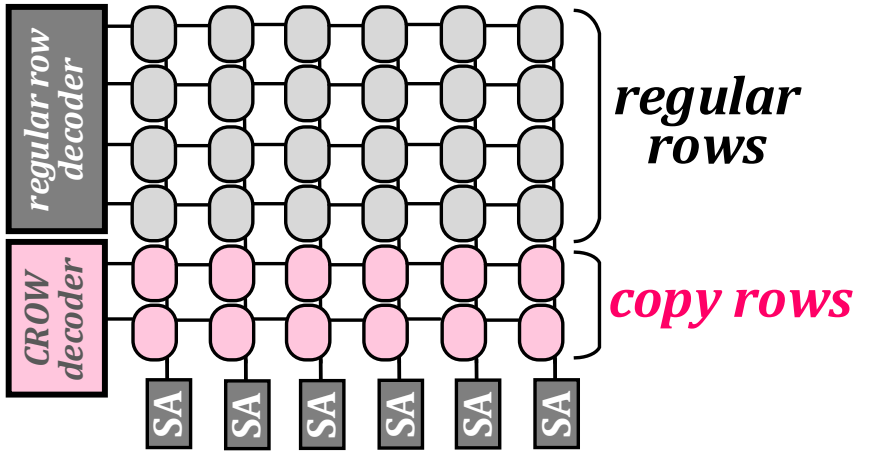

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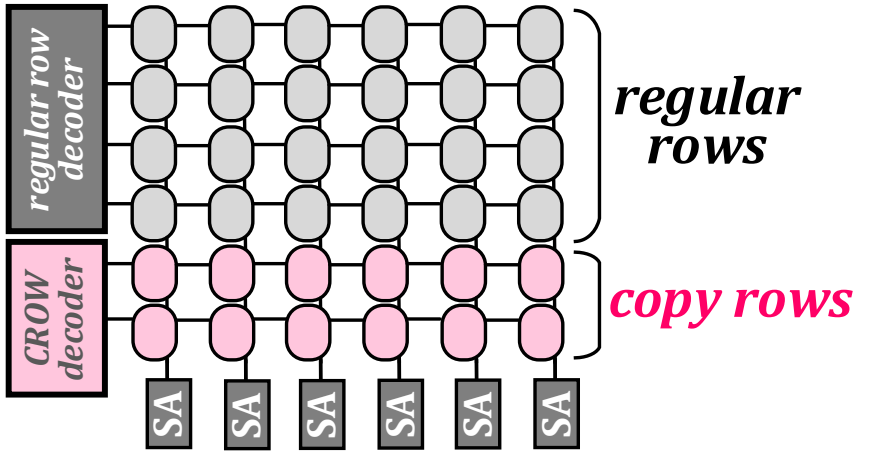

CROW is a flexible substrate with many use cases:

- CROW-cache & CROW-ref **(20% speedup** and consumes **22% less DRAM energy)**

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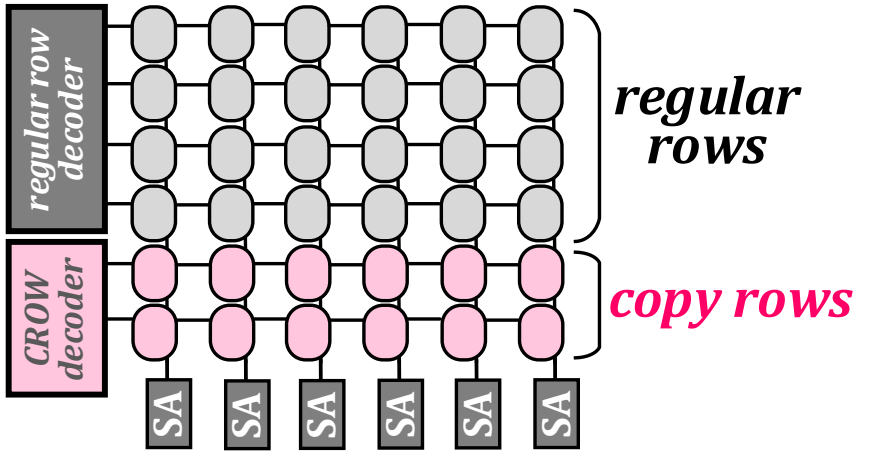

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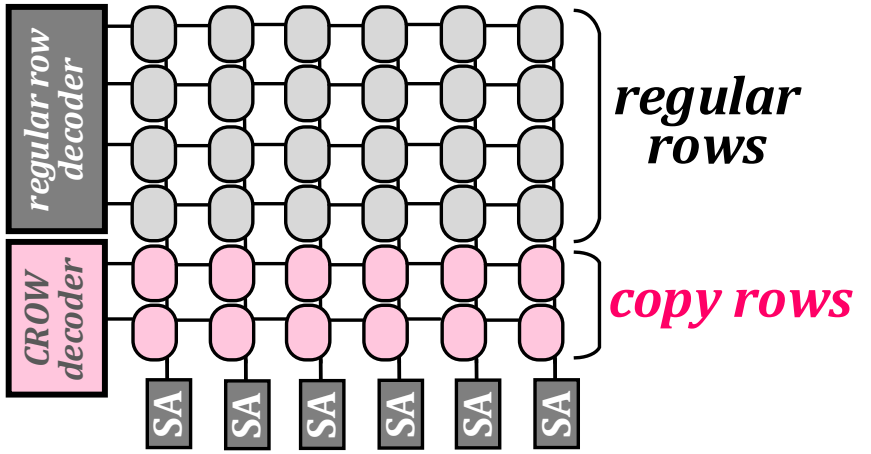

CROW is a flexible substrate with many use cases:

- CROW-cache & CROW-ref **(20% speedup** and consumes **22% less DRAM energy)**
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- We hope CROW enables many other use cases going forward

CROW

A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability

Hasan Hassan

Minesh Patel *Jeremie S. Kim* *A. Giray Yaglikci* *Nandita Vijaykumar*

Nika Mansouri Ghiasi *Saugata Ghose* *Onur Mutlu*

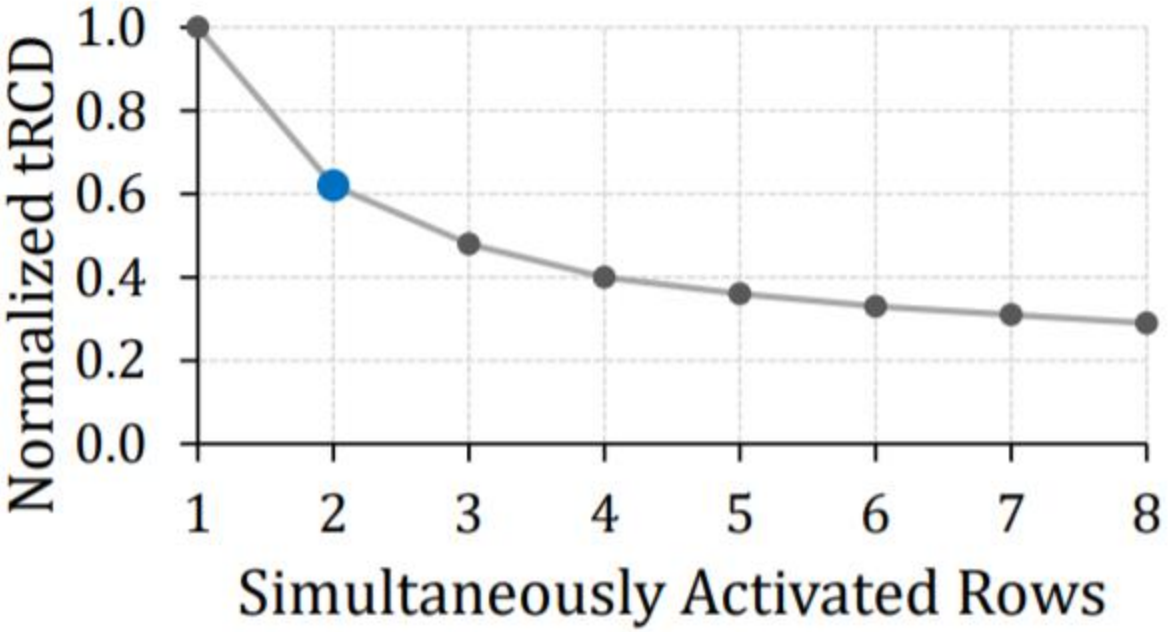
ETH zürich

Carnegie Mellon University

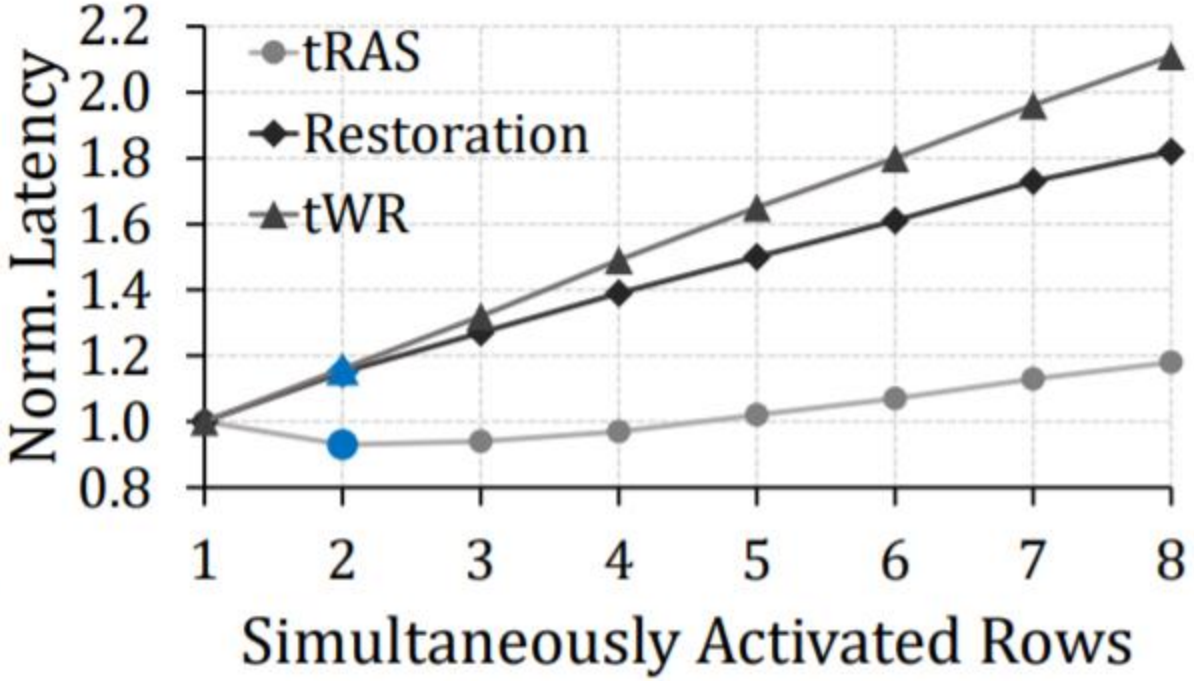
SAFARI

Backup Slides

Latency Reduction with MRA



(a) **tRCD** (18 ns)



(b) **tRAS** (42 ns), **tWR** (18 ns), **and restoration** (24 ns)

Mitigating RowHammer

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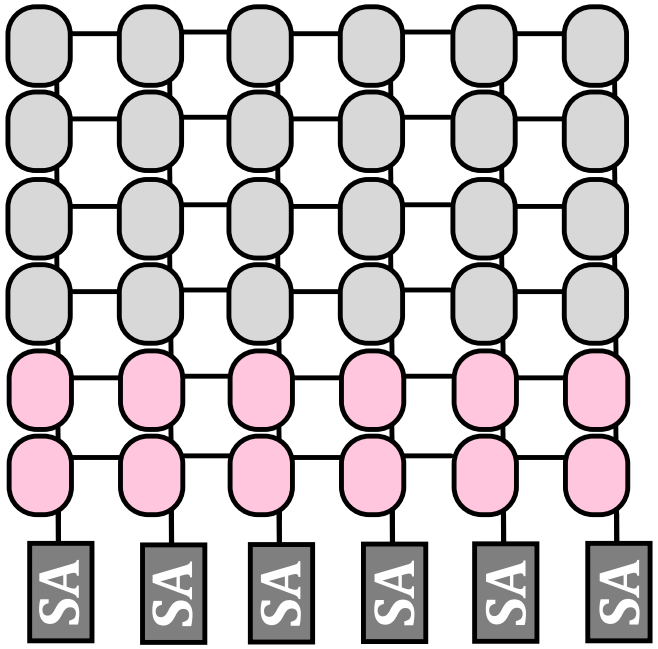

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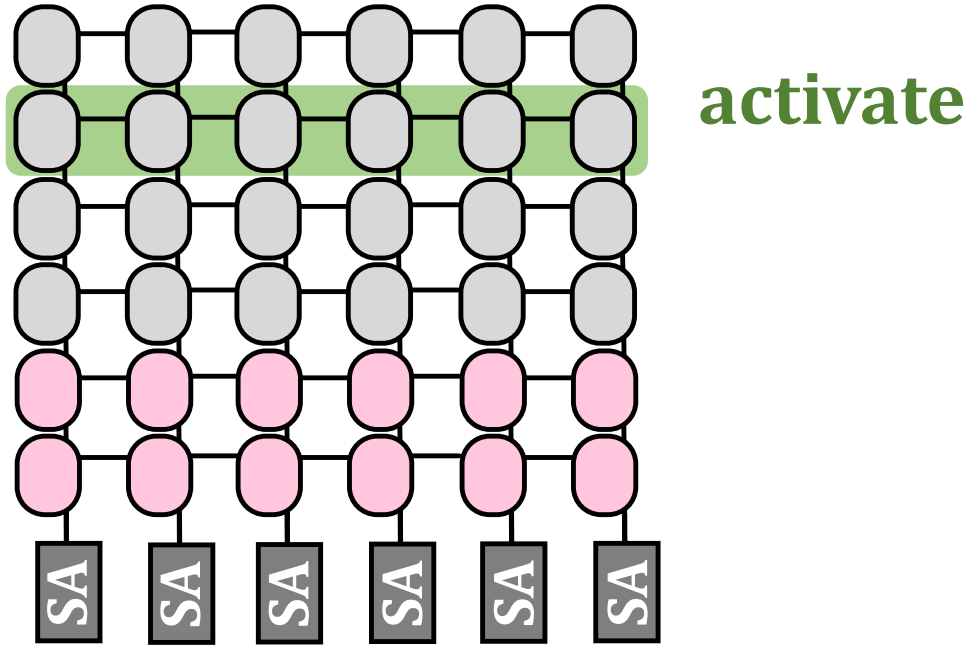

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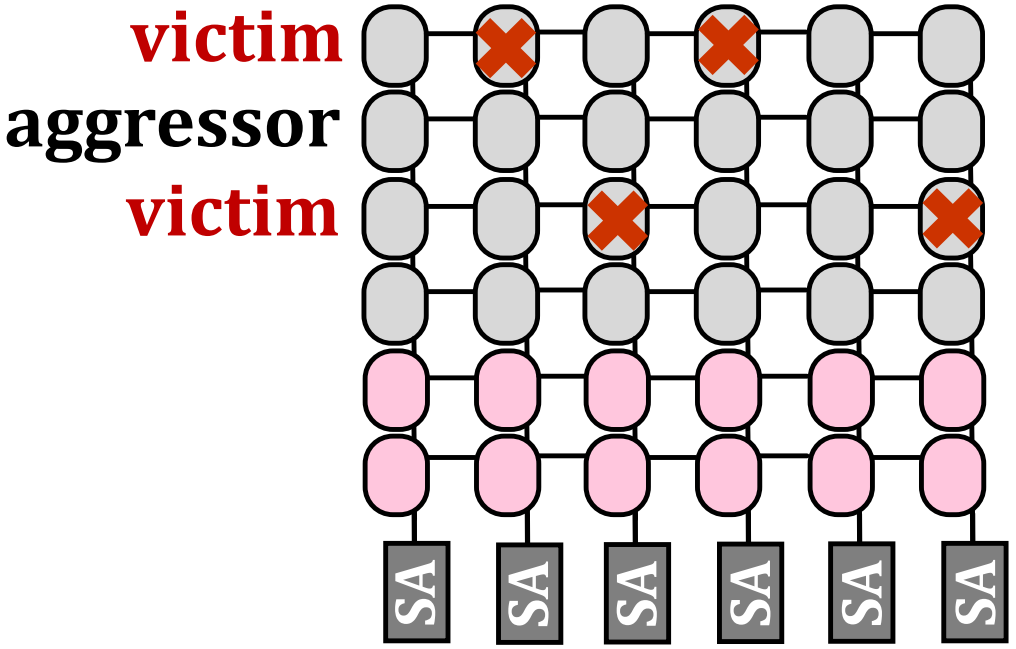

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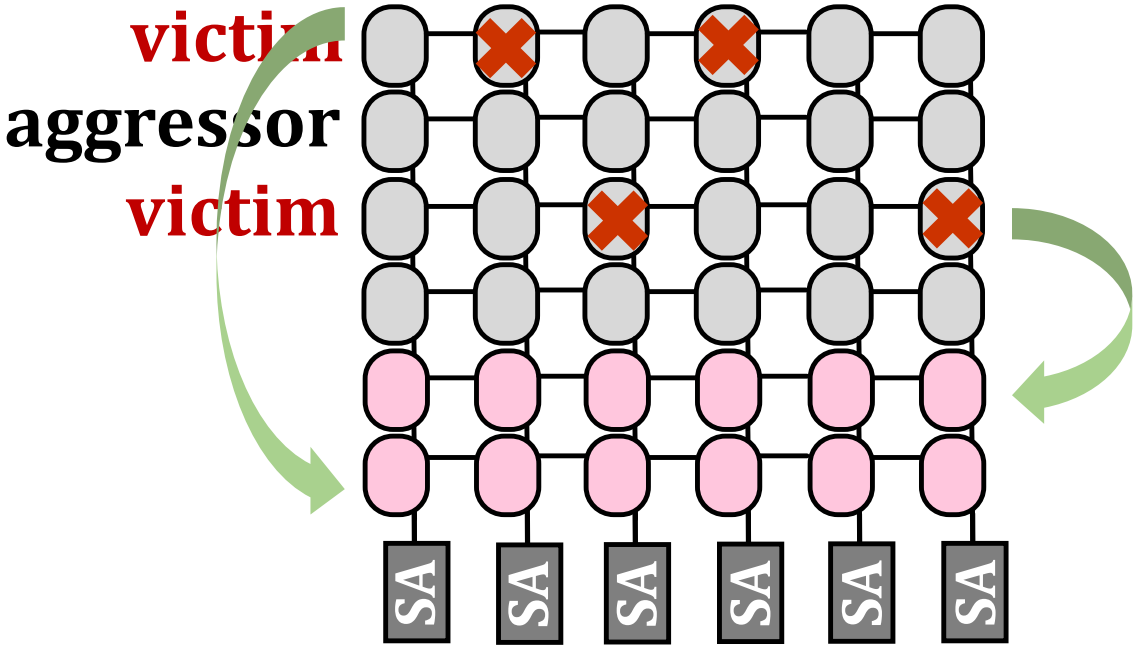

Key idea: remap victim rows to copy rows

CROW-cache Performance

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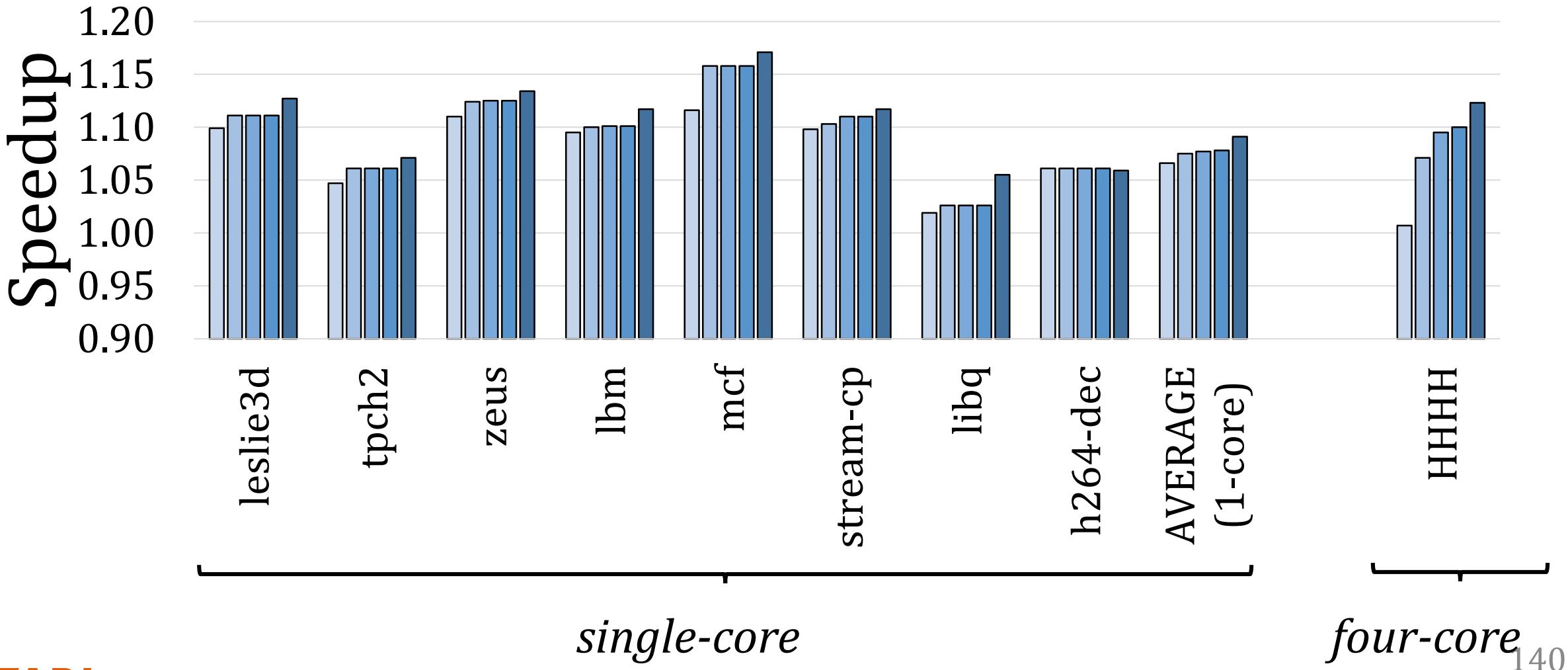

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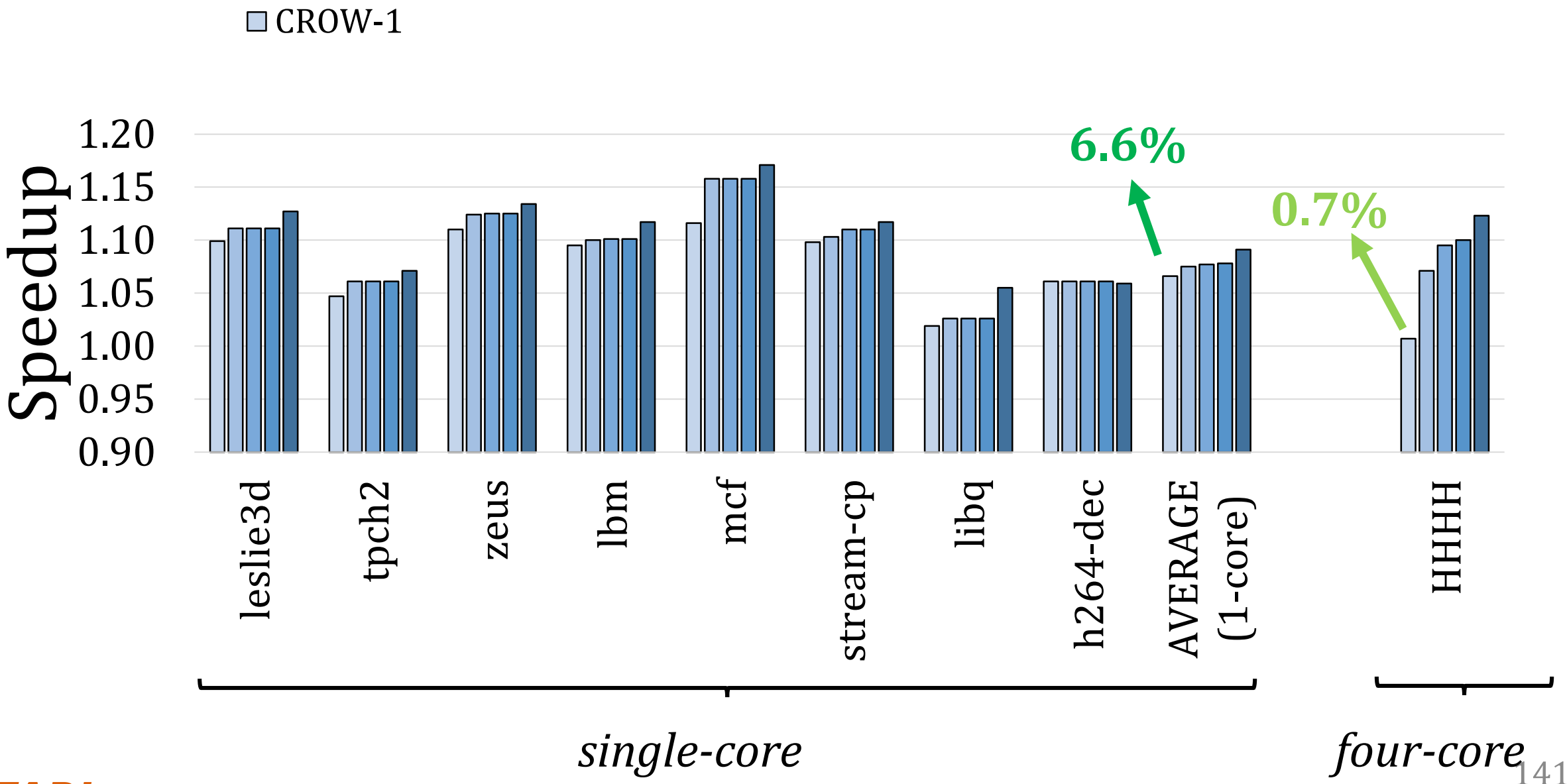

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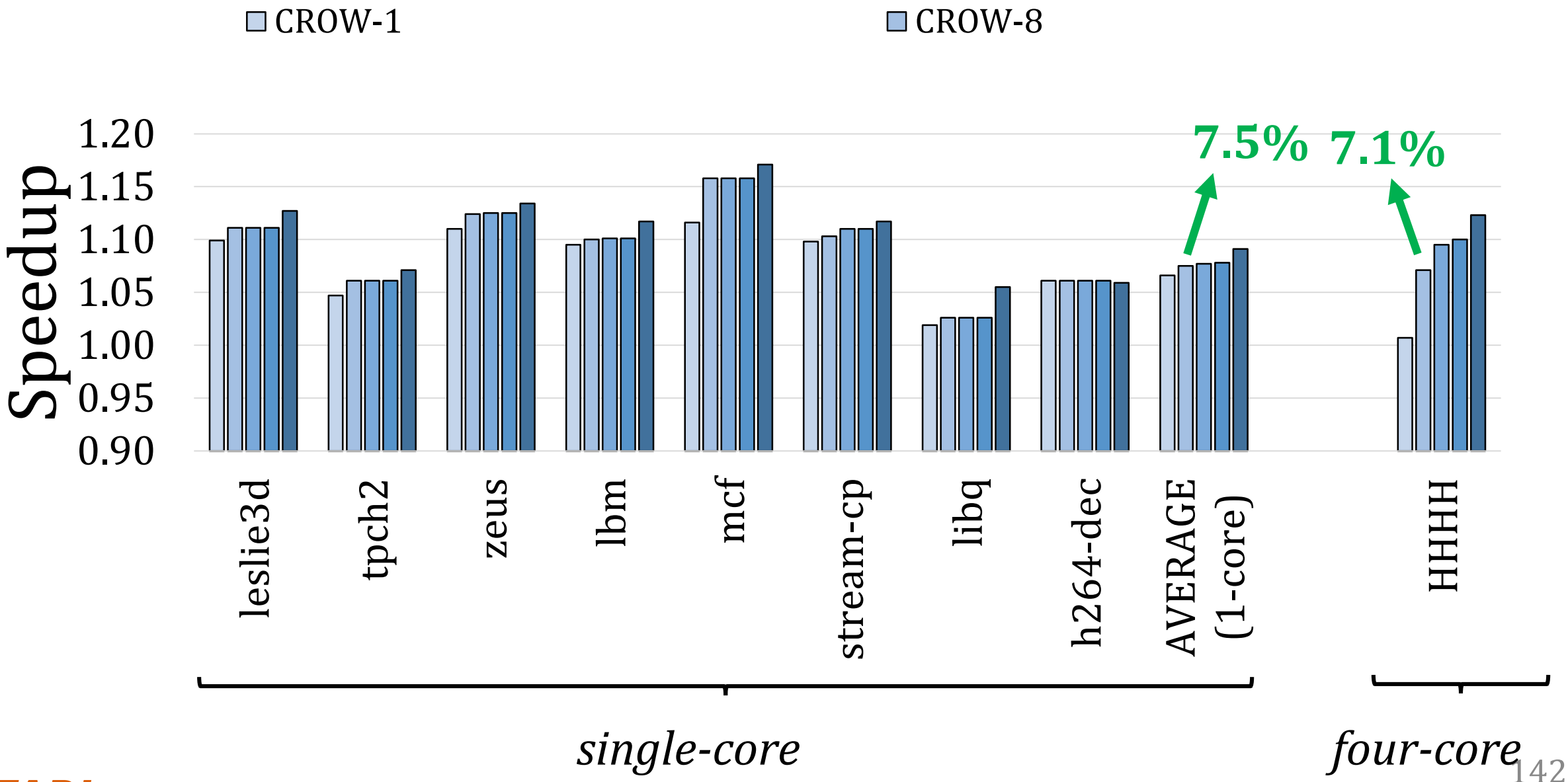

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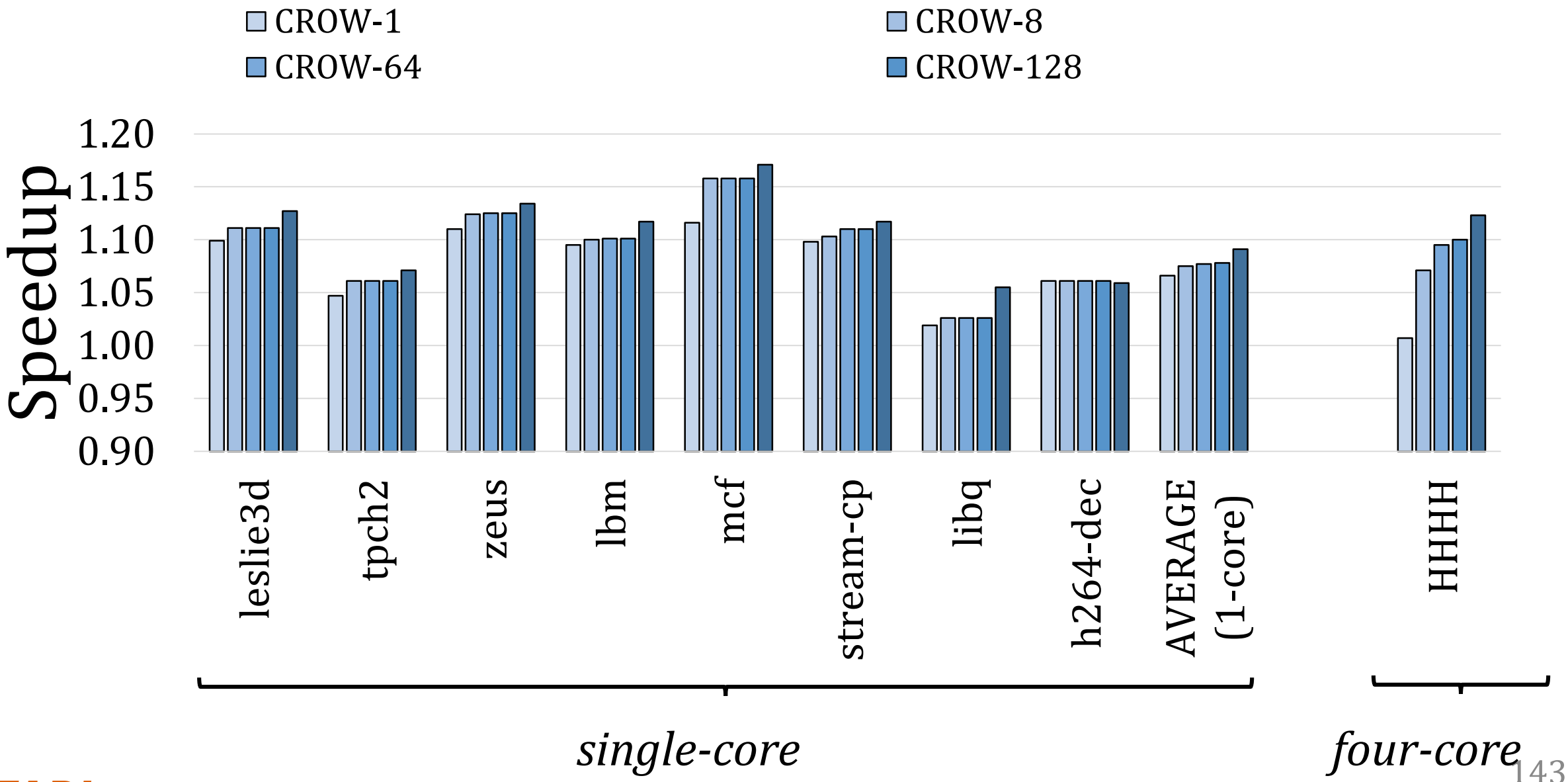

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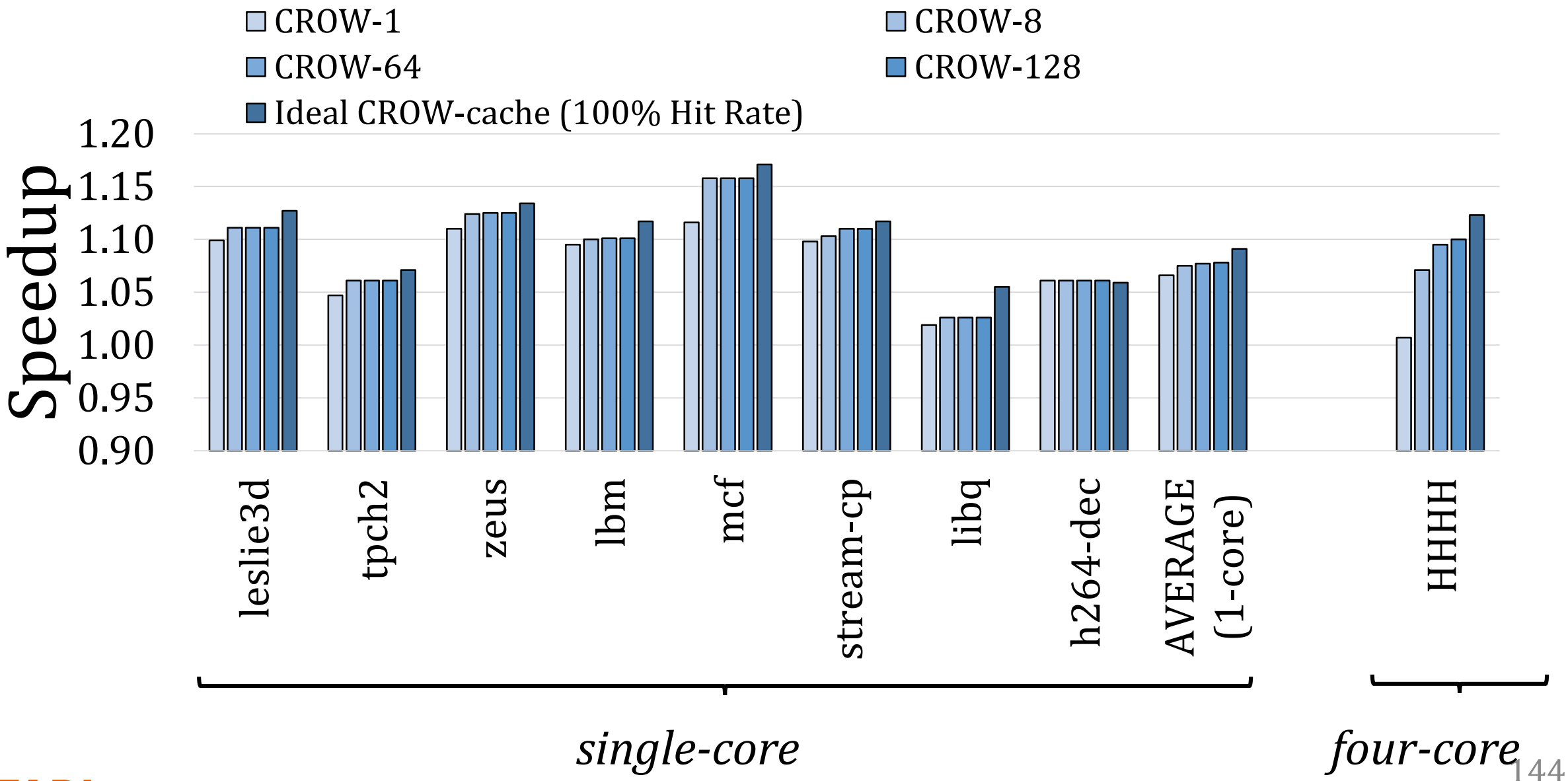

CROW-ref Performance

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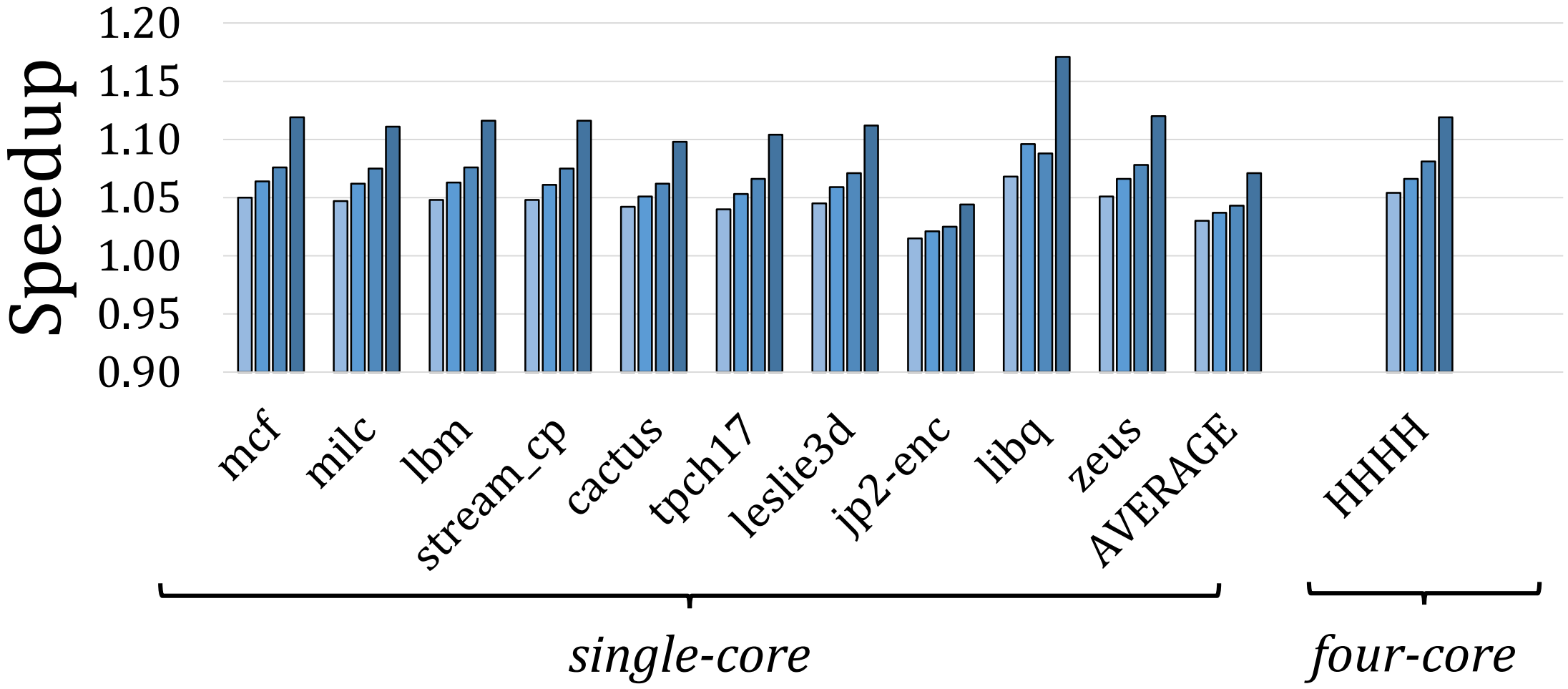
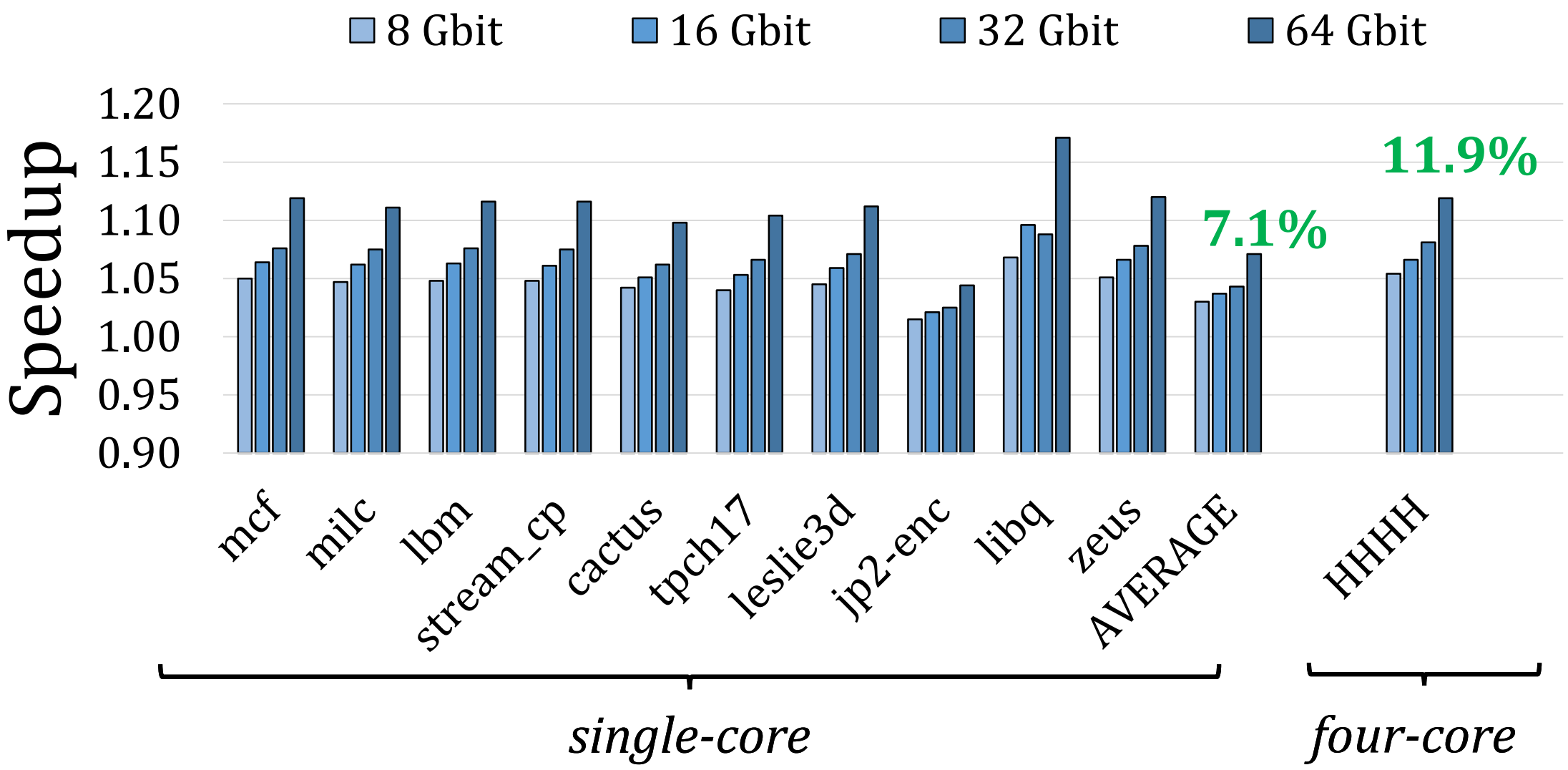


CROW-ref Performance



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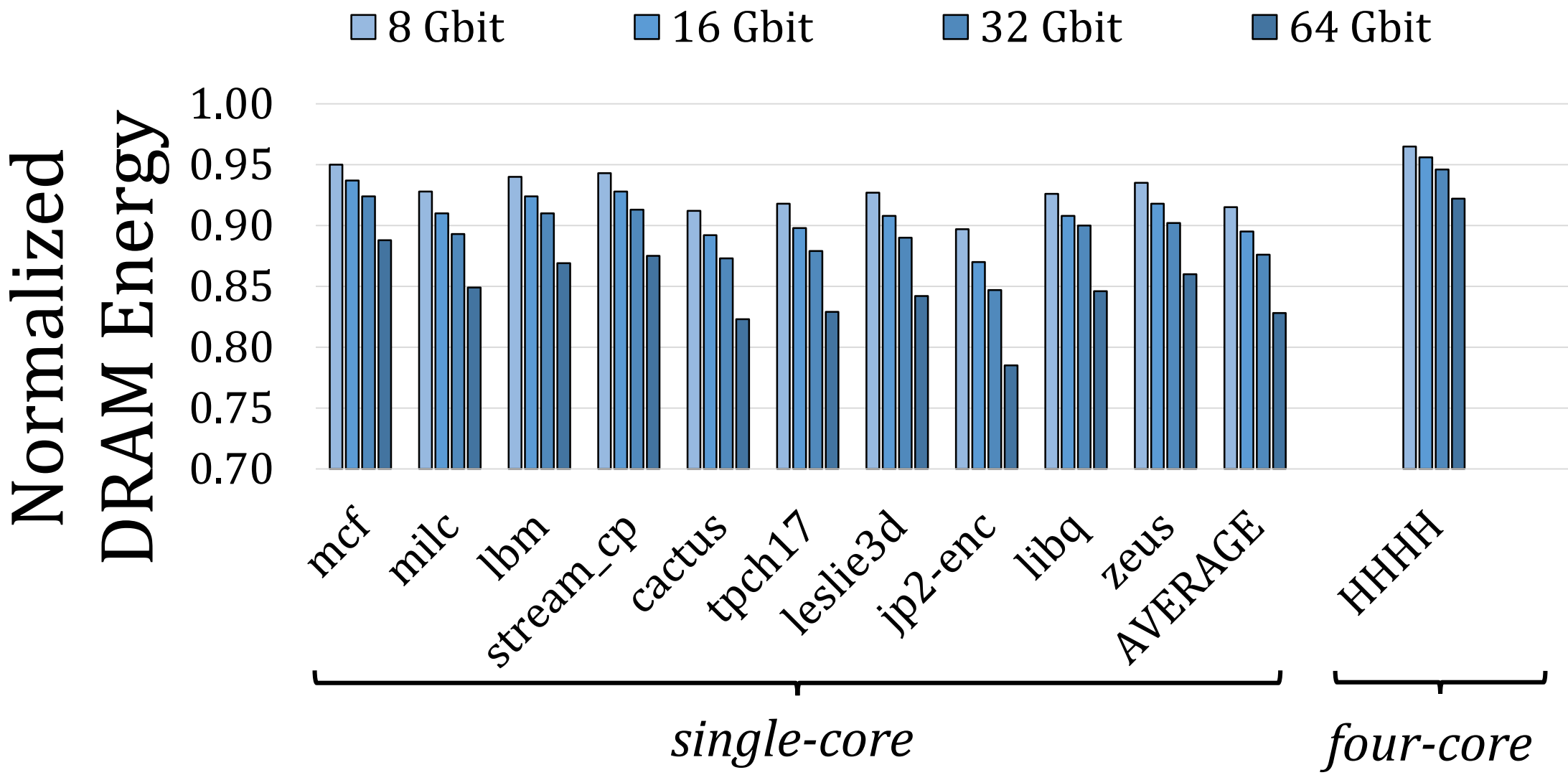
CROW-ref Energy Savings



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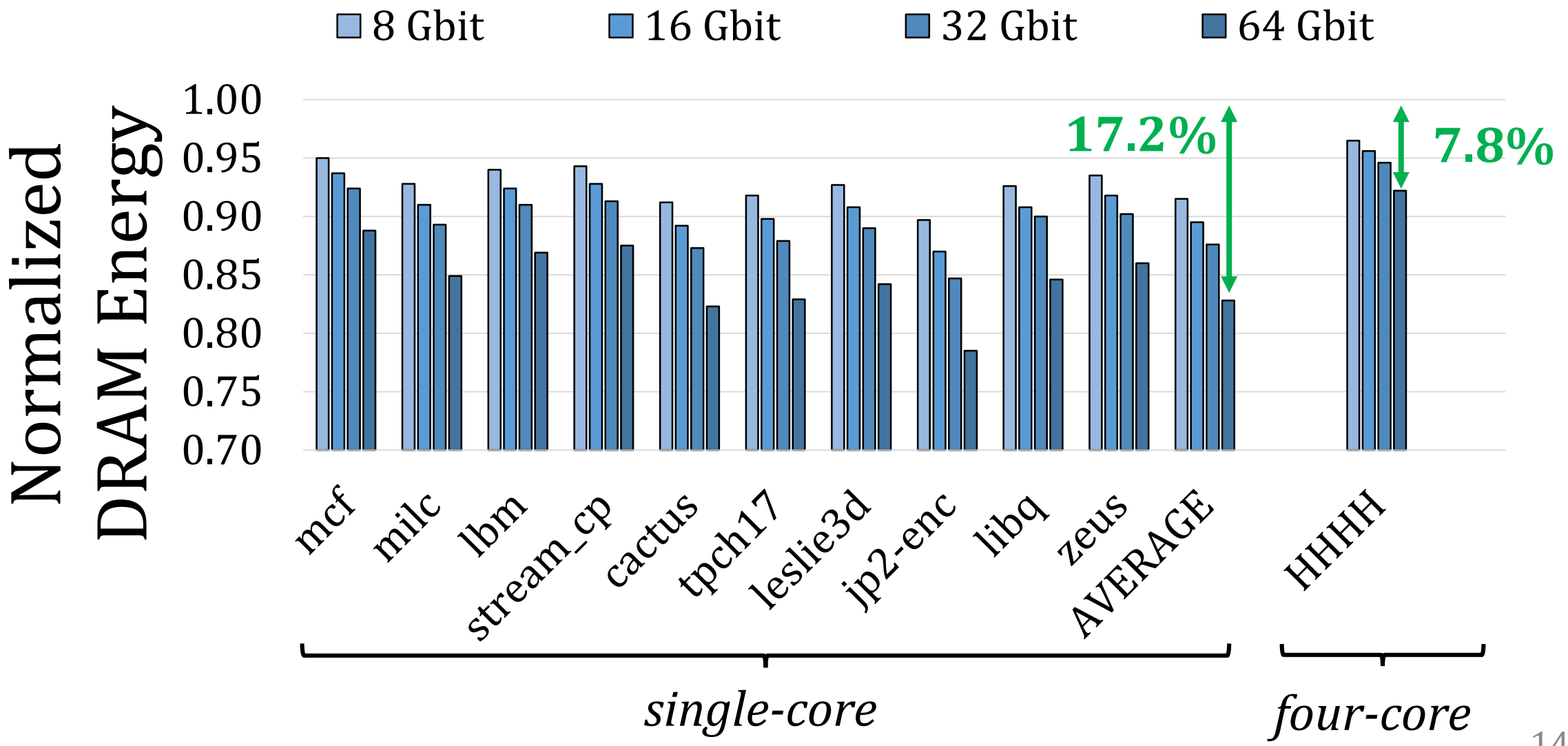
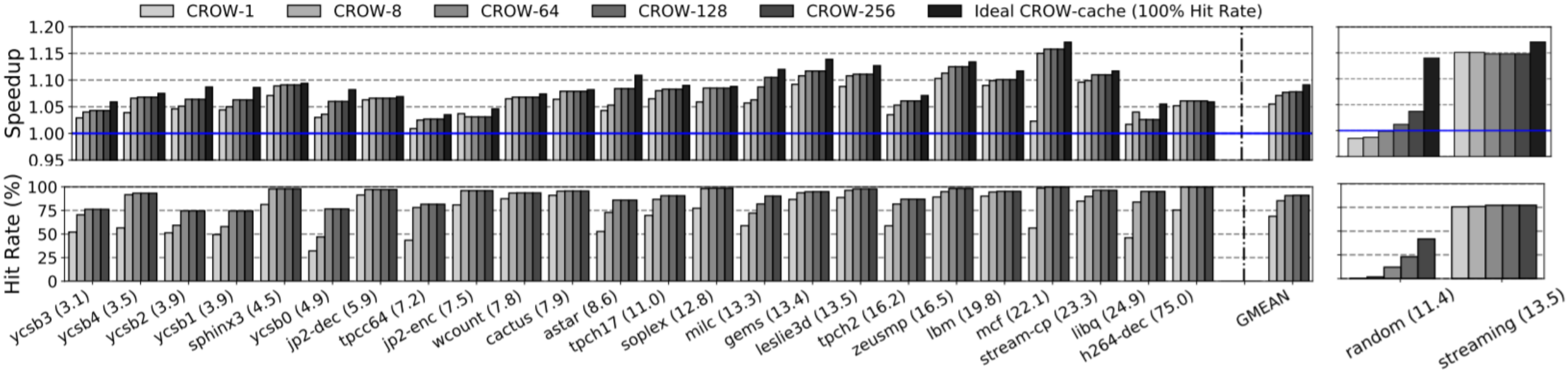


SAFARI

Speedup - CROW-cache

Single-core



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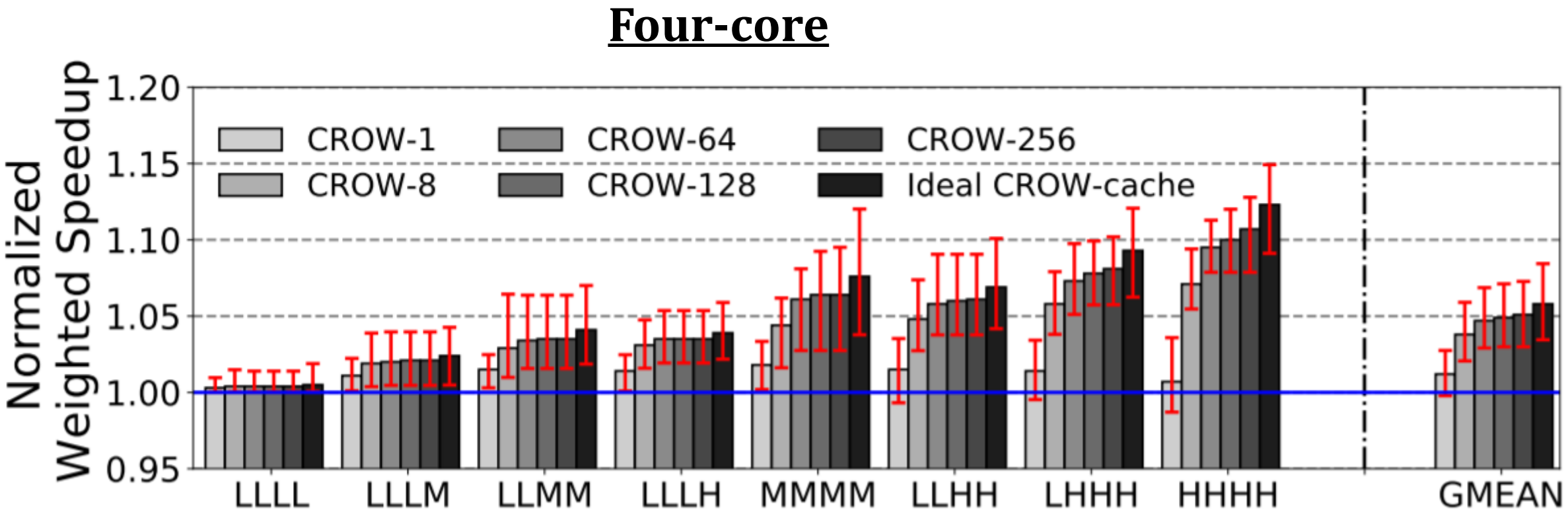
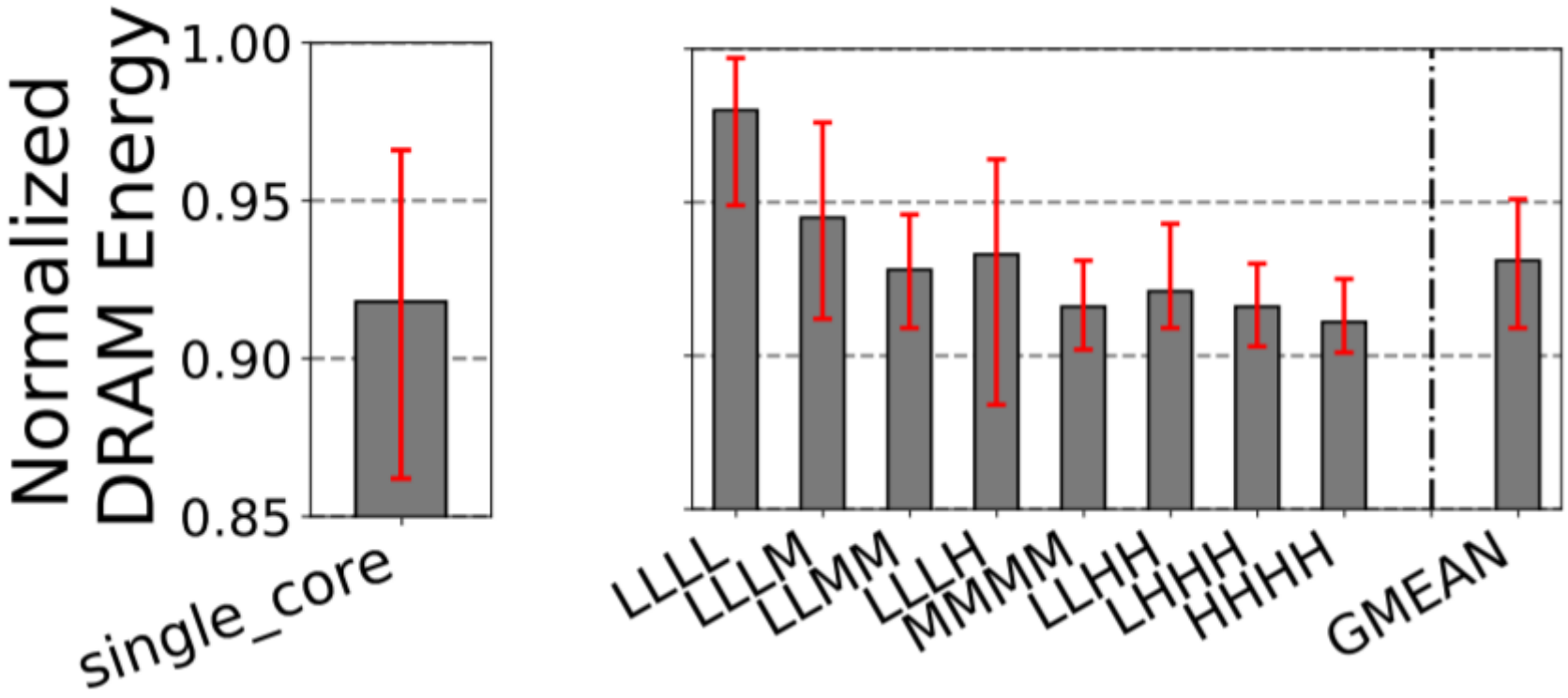
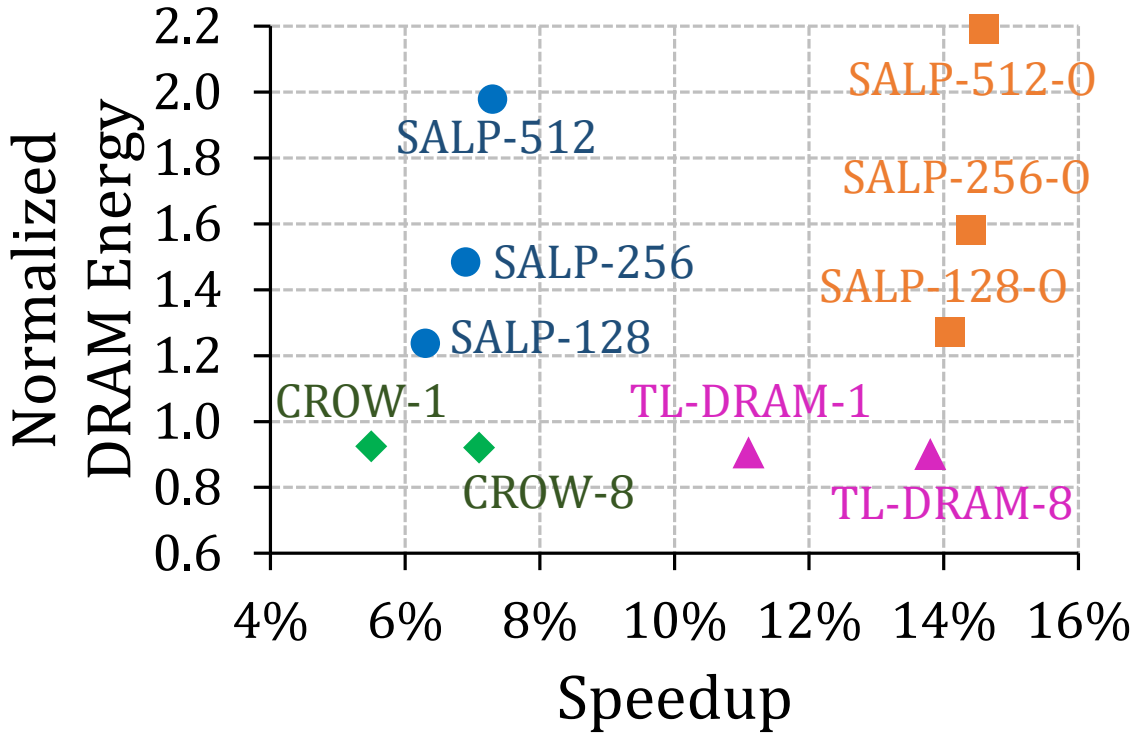
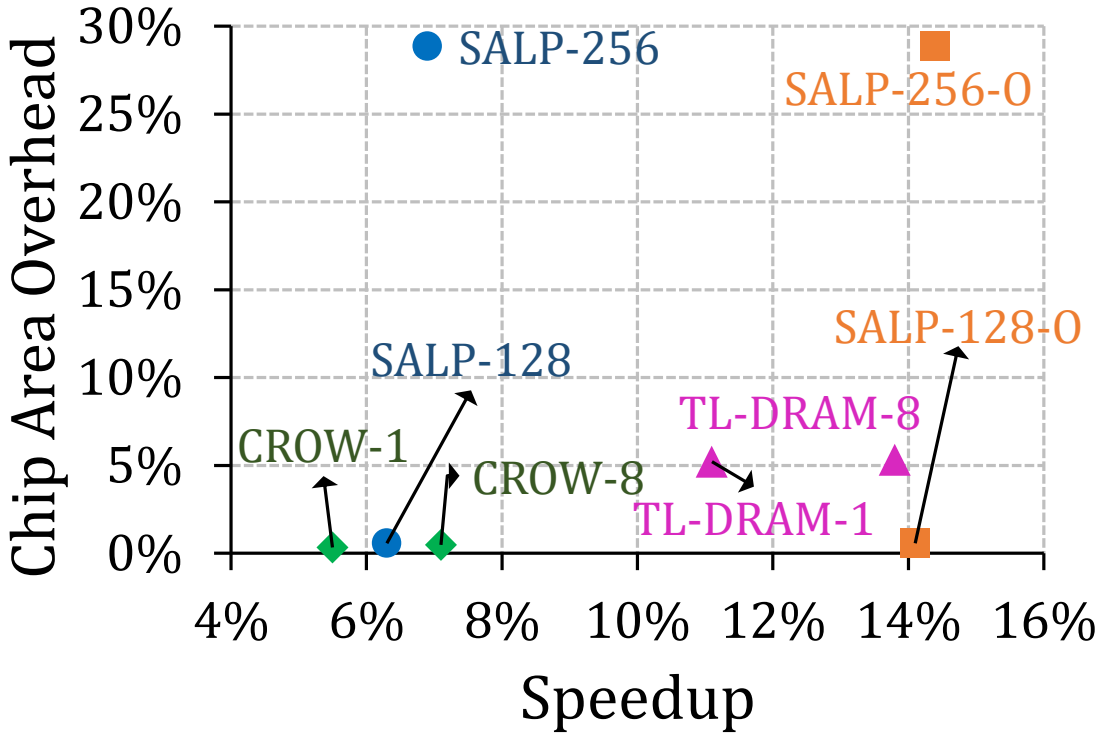


Energy – CROW-cache

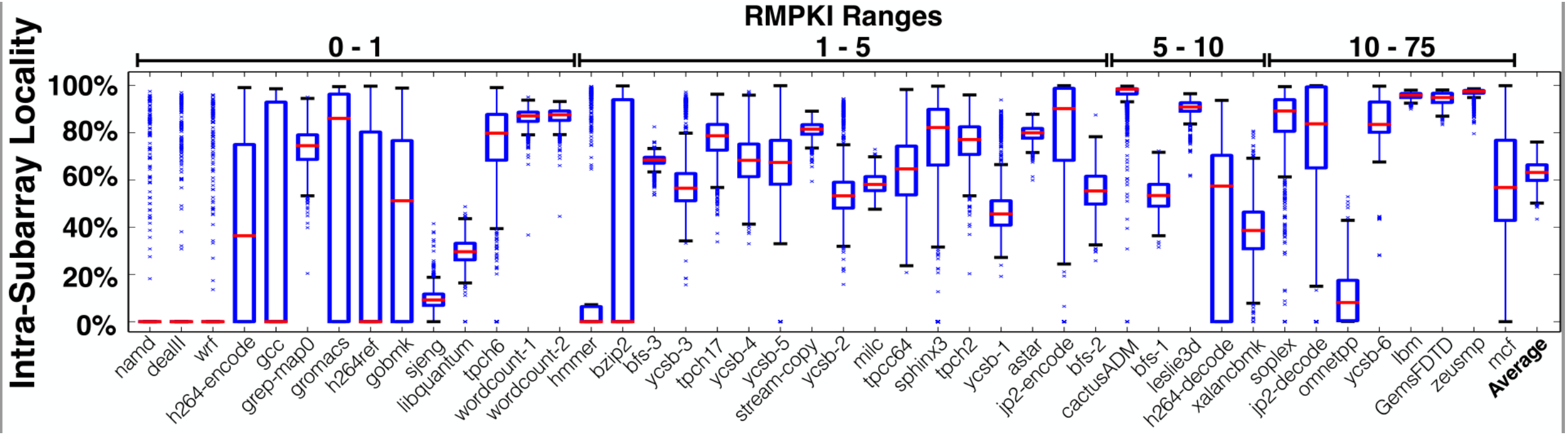


Comparison to TL-DRAM and SALP

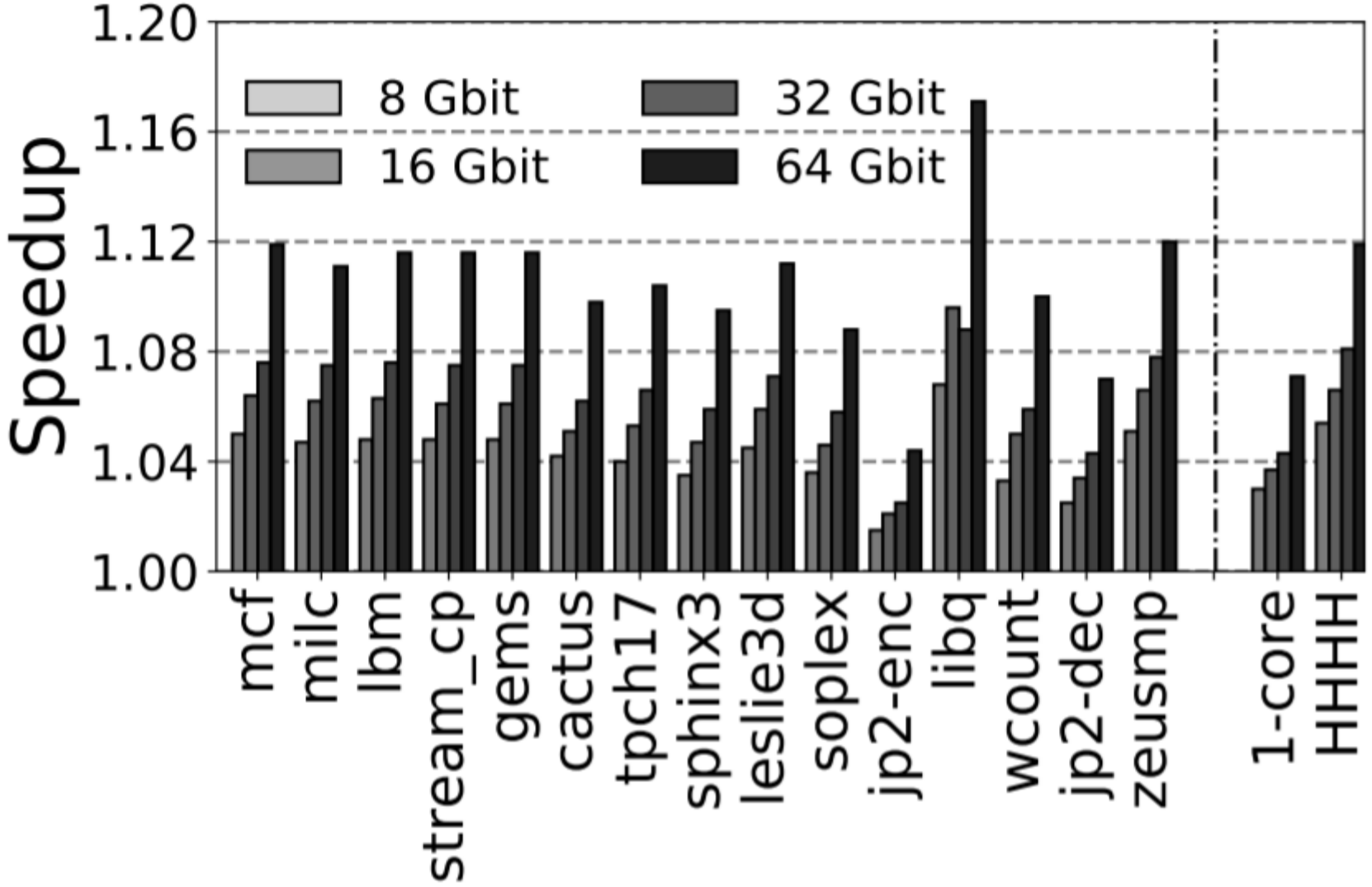




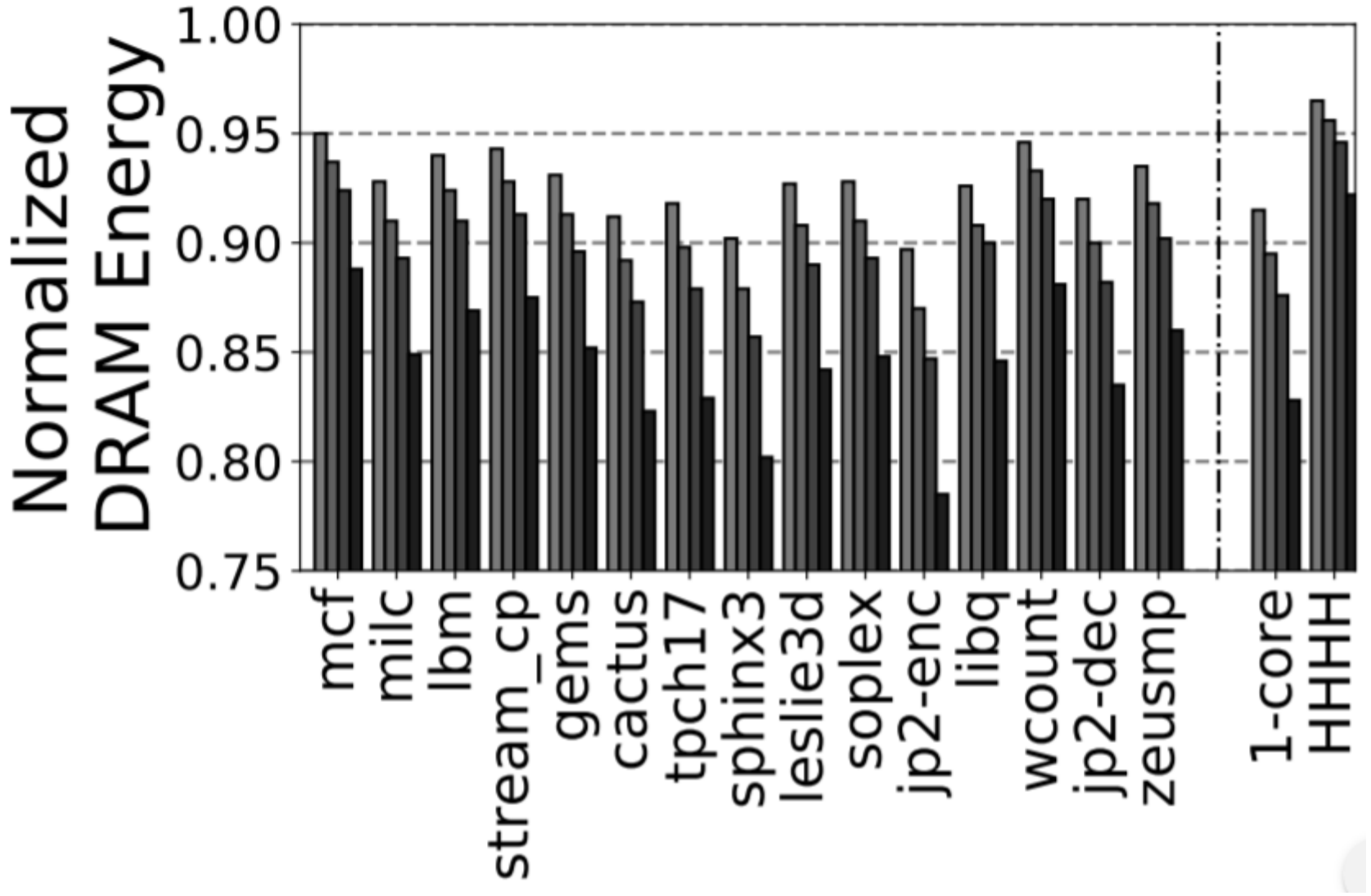
Slide on RLTL



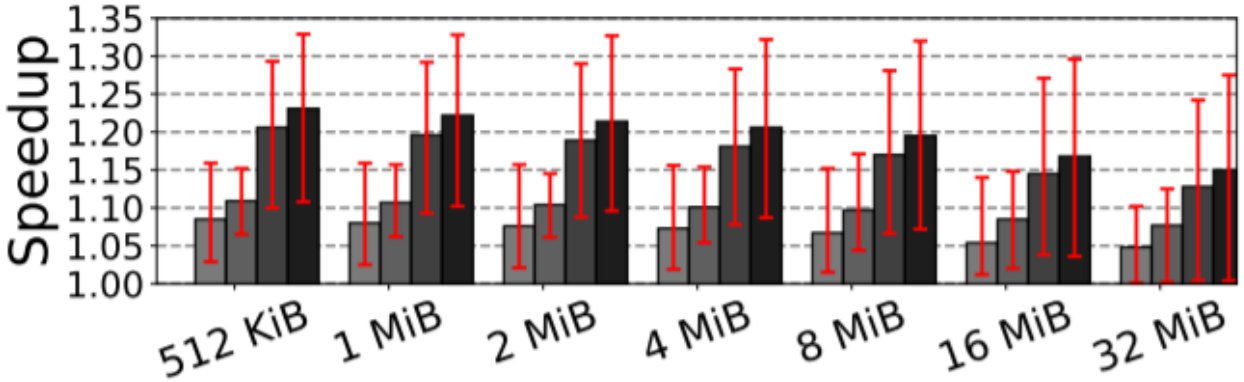
Speedup – CROW-ref

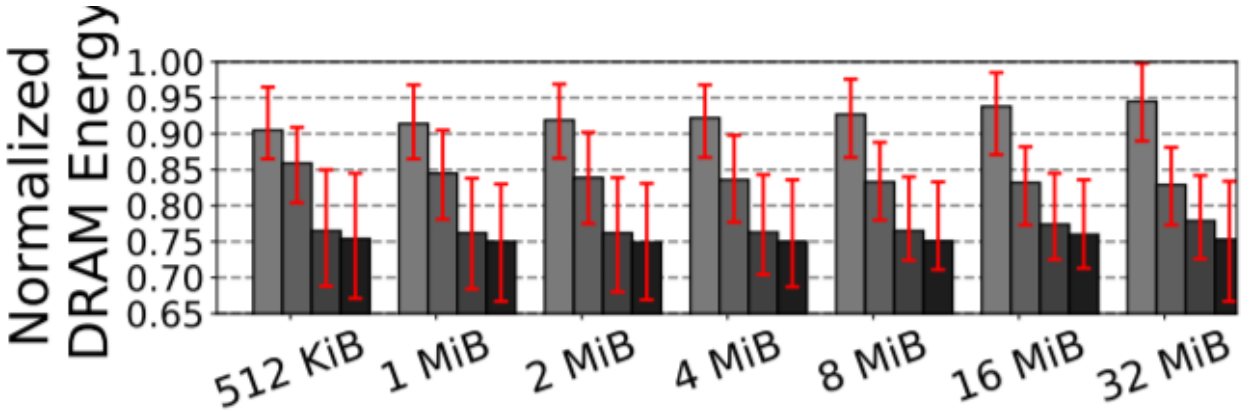


Energy – CROW-ref

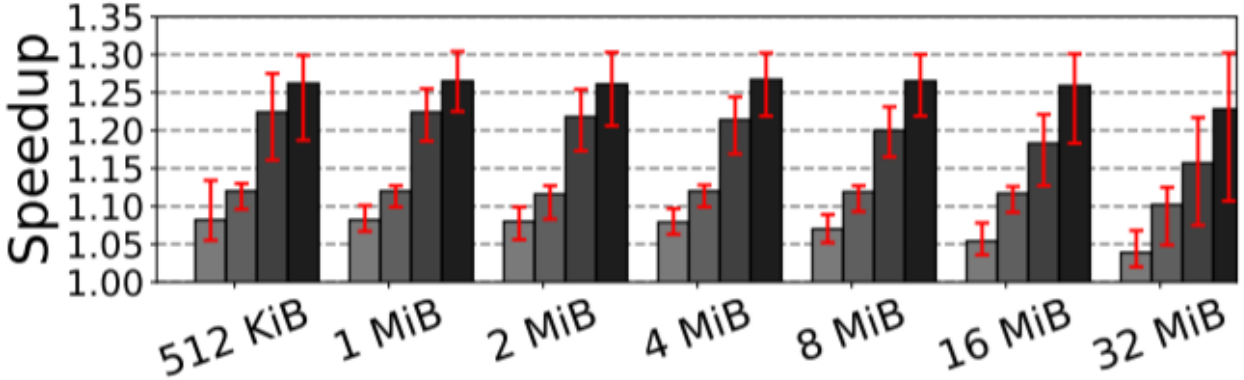


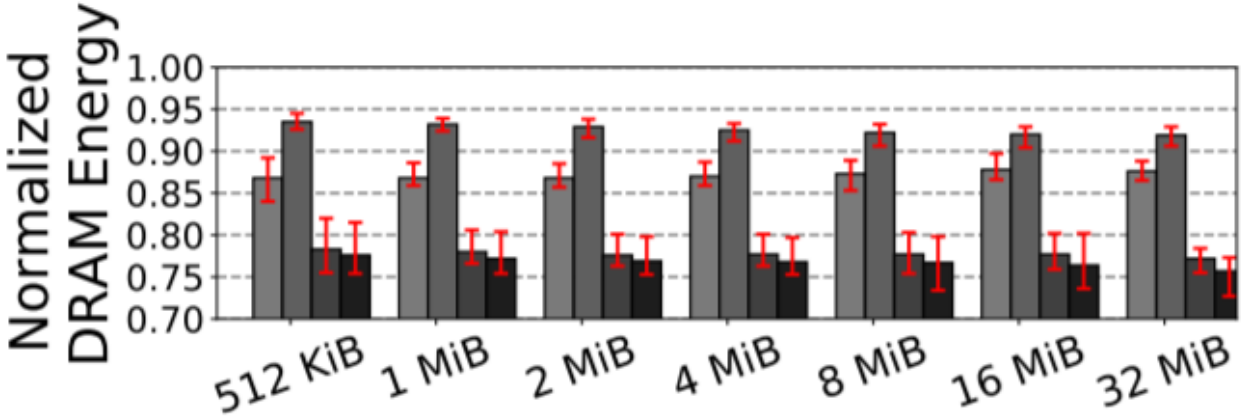
CROW-cache + ref





(a) Single-core workloads





(b) Four-core workloads

CROW-table Organization

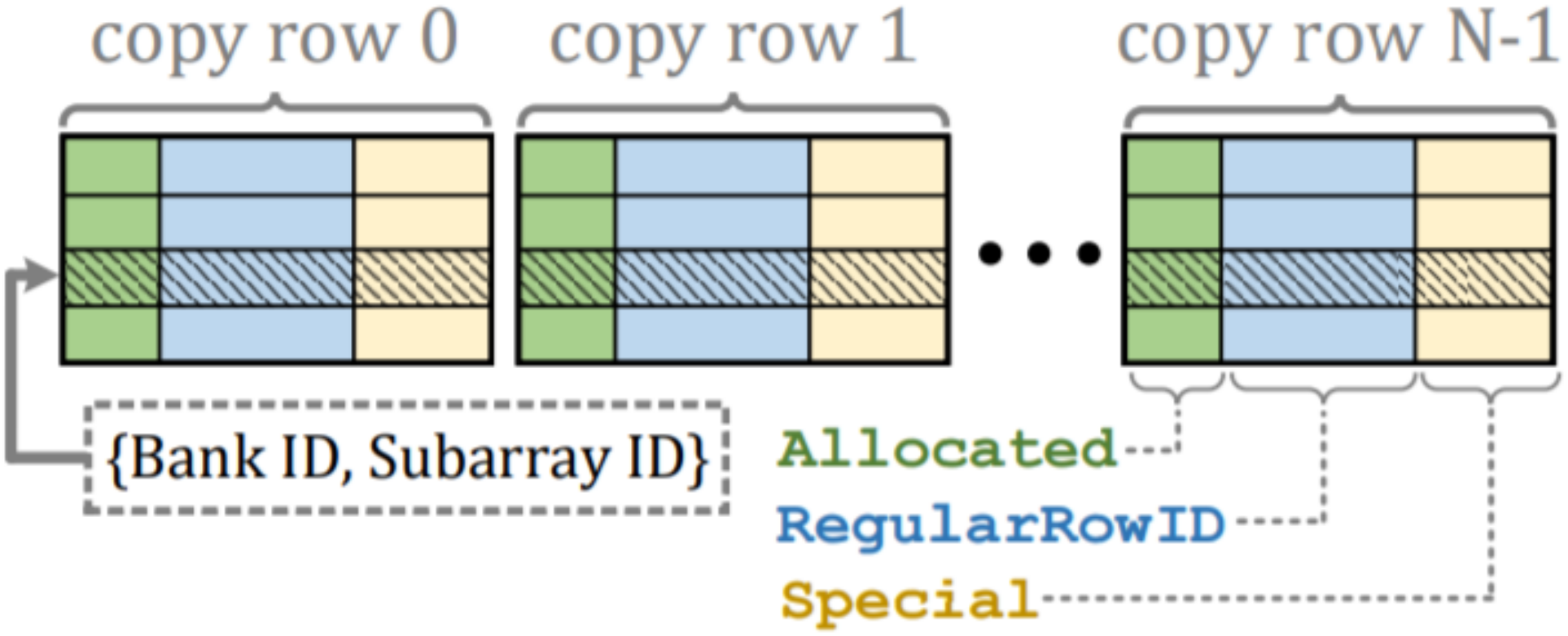


Figure 4: Organization of the CROW-table.

tRCD vs tRAS

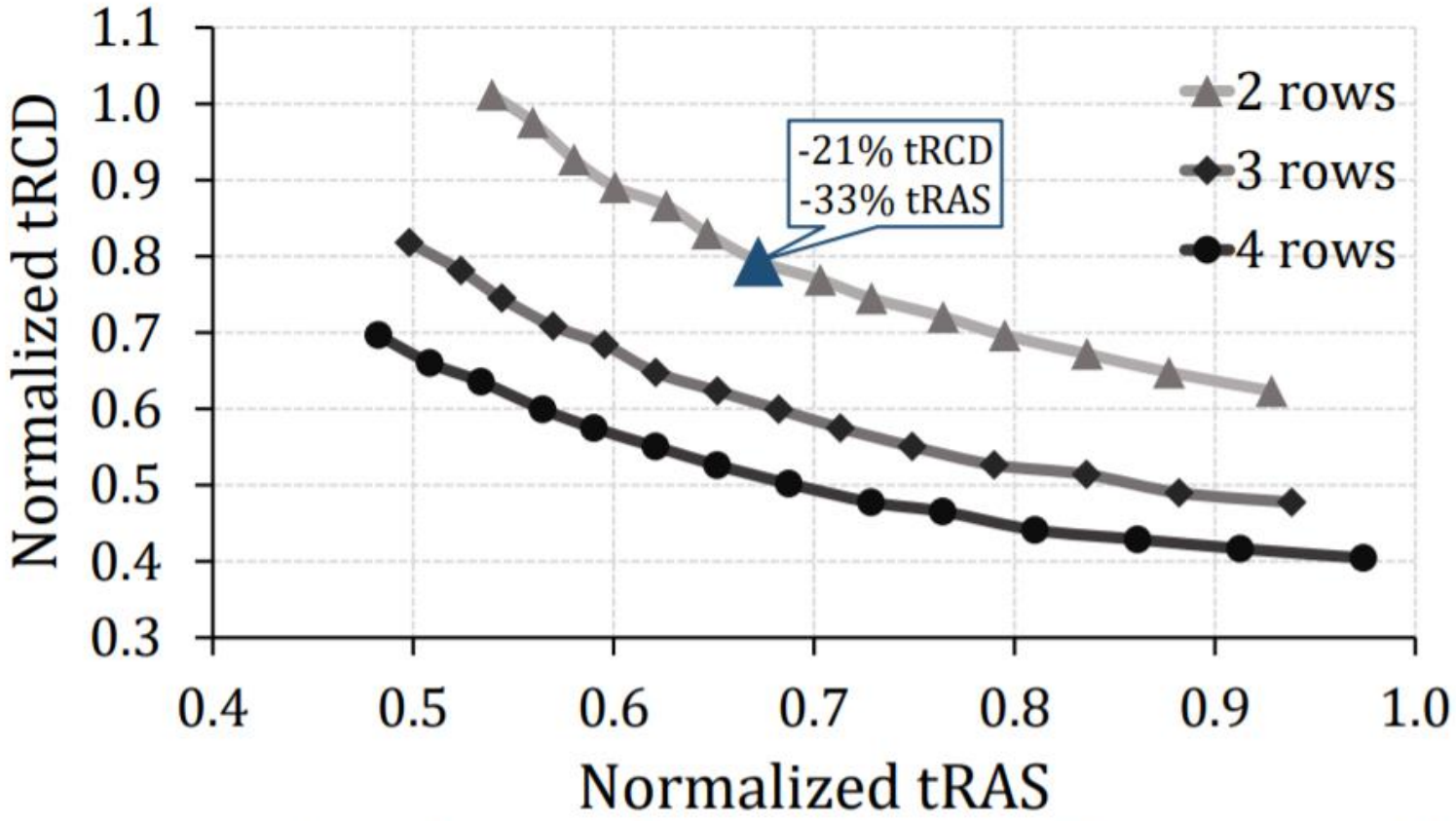


Figure 6: Normalized tRCD latency as a function of normalized tRAS latency for different number of simultaneously activated DRAM rows.

MRA Area Overhead

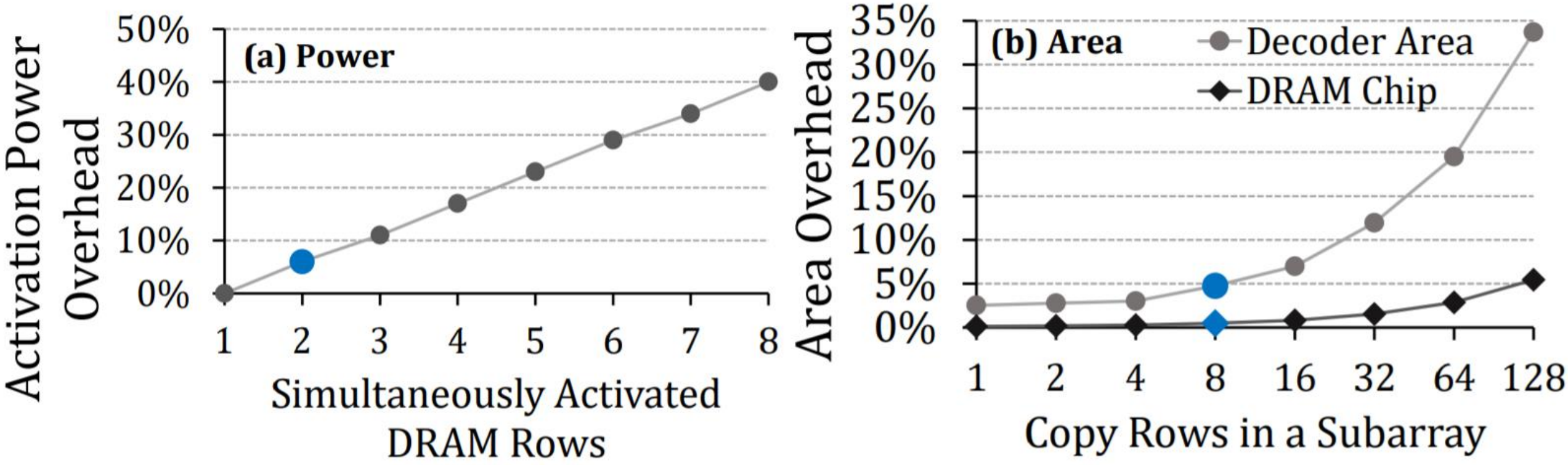
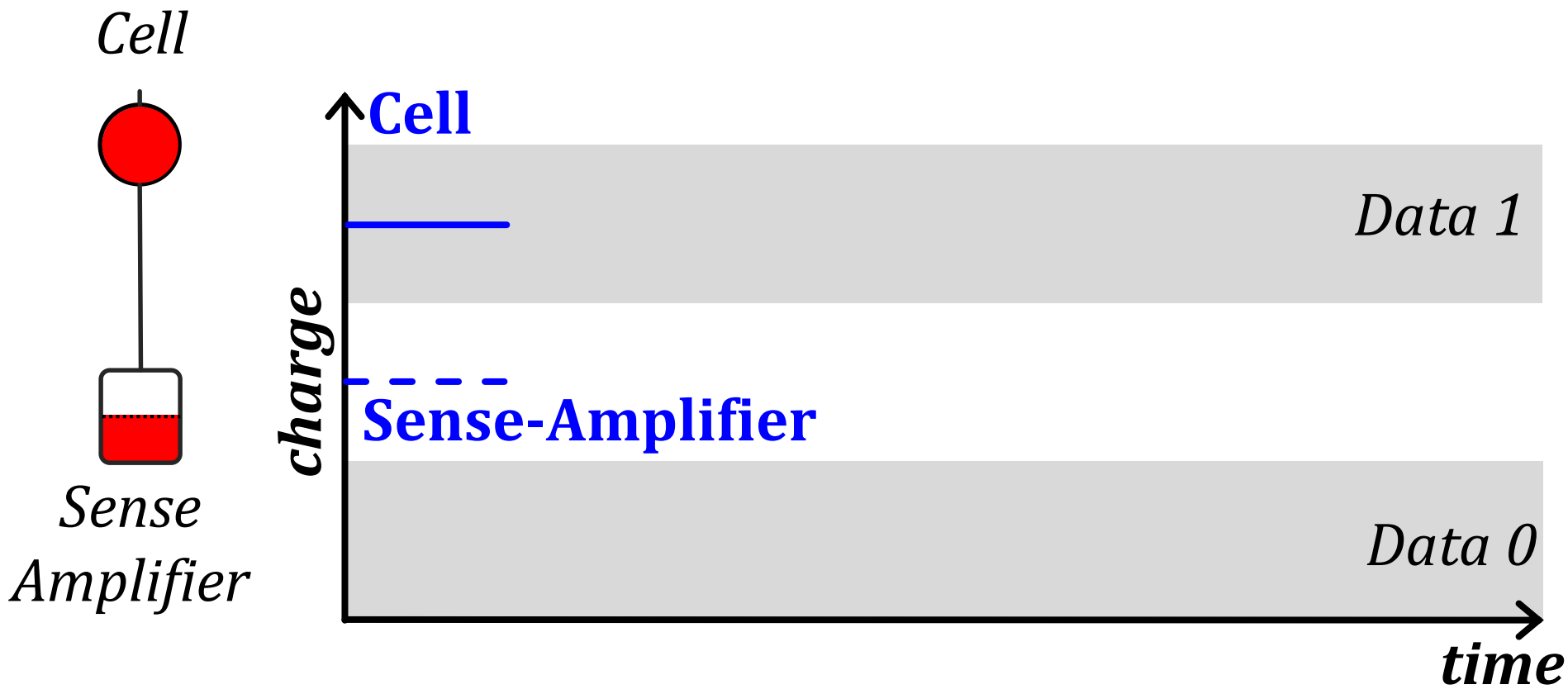
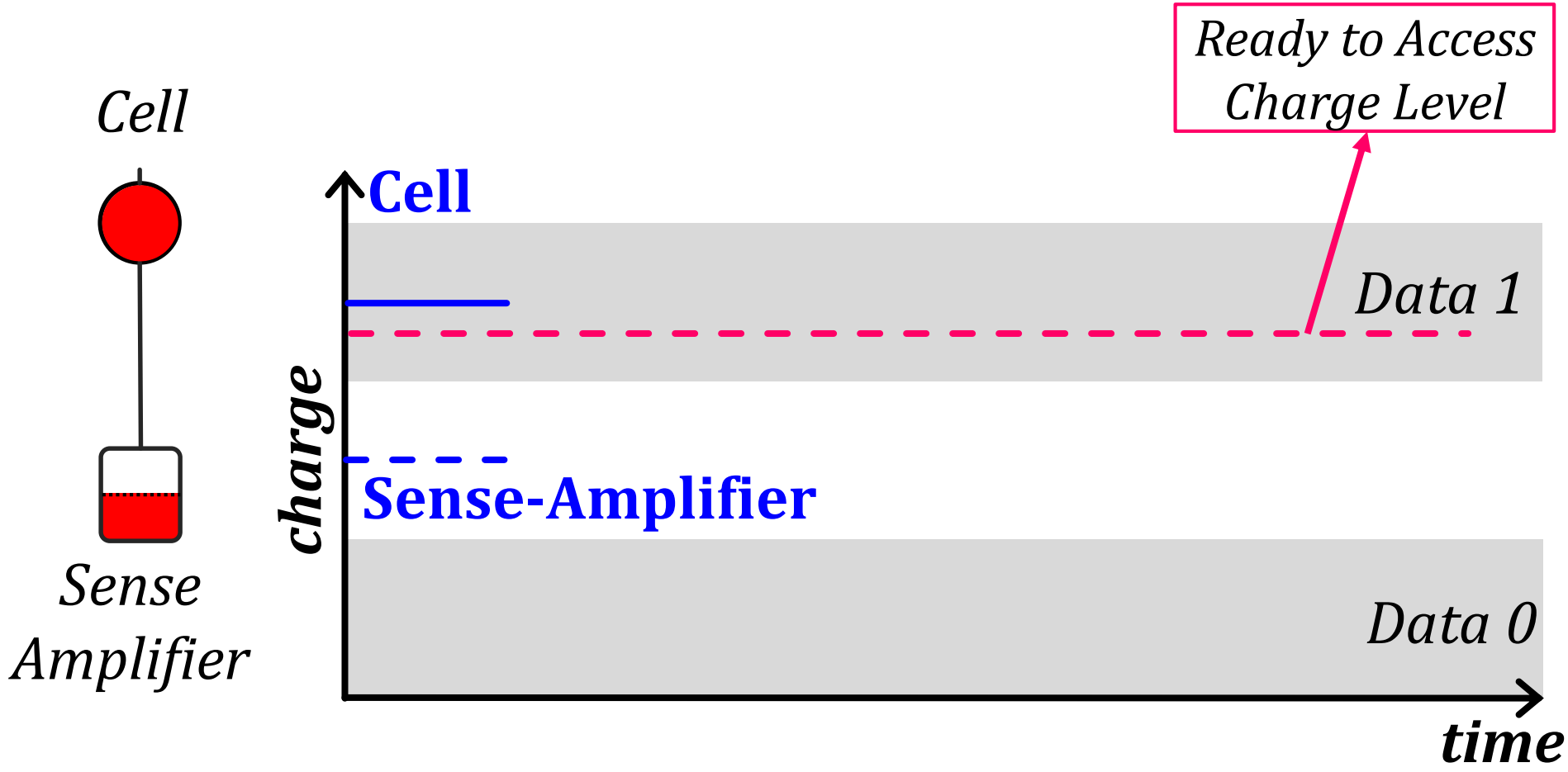


Figure 7: Power consumption and area overhead of MRA.

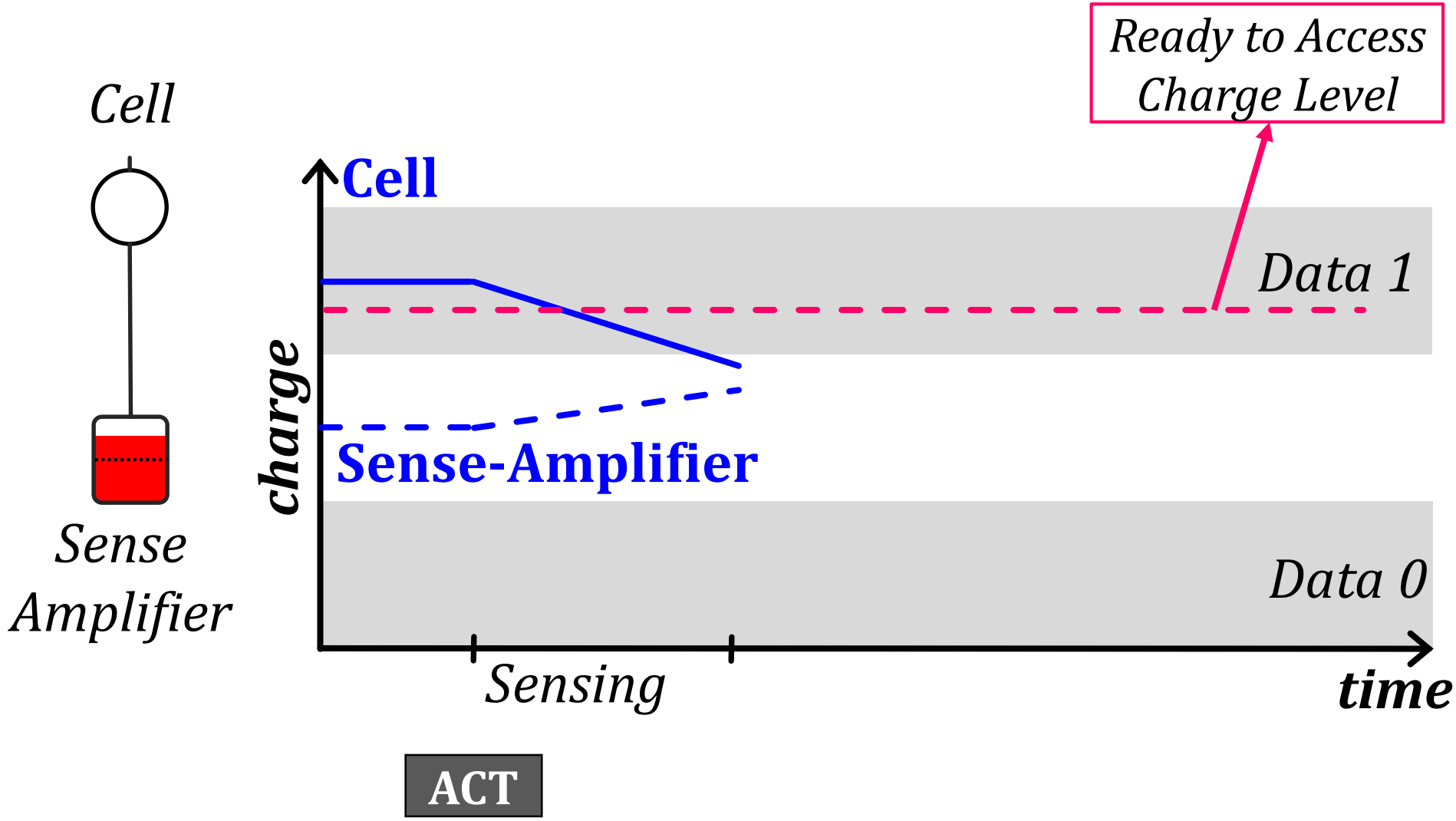
DRAM Charge over Time



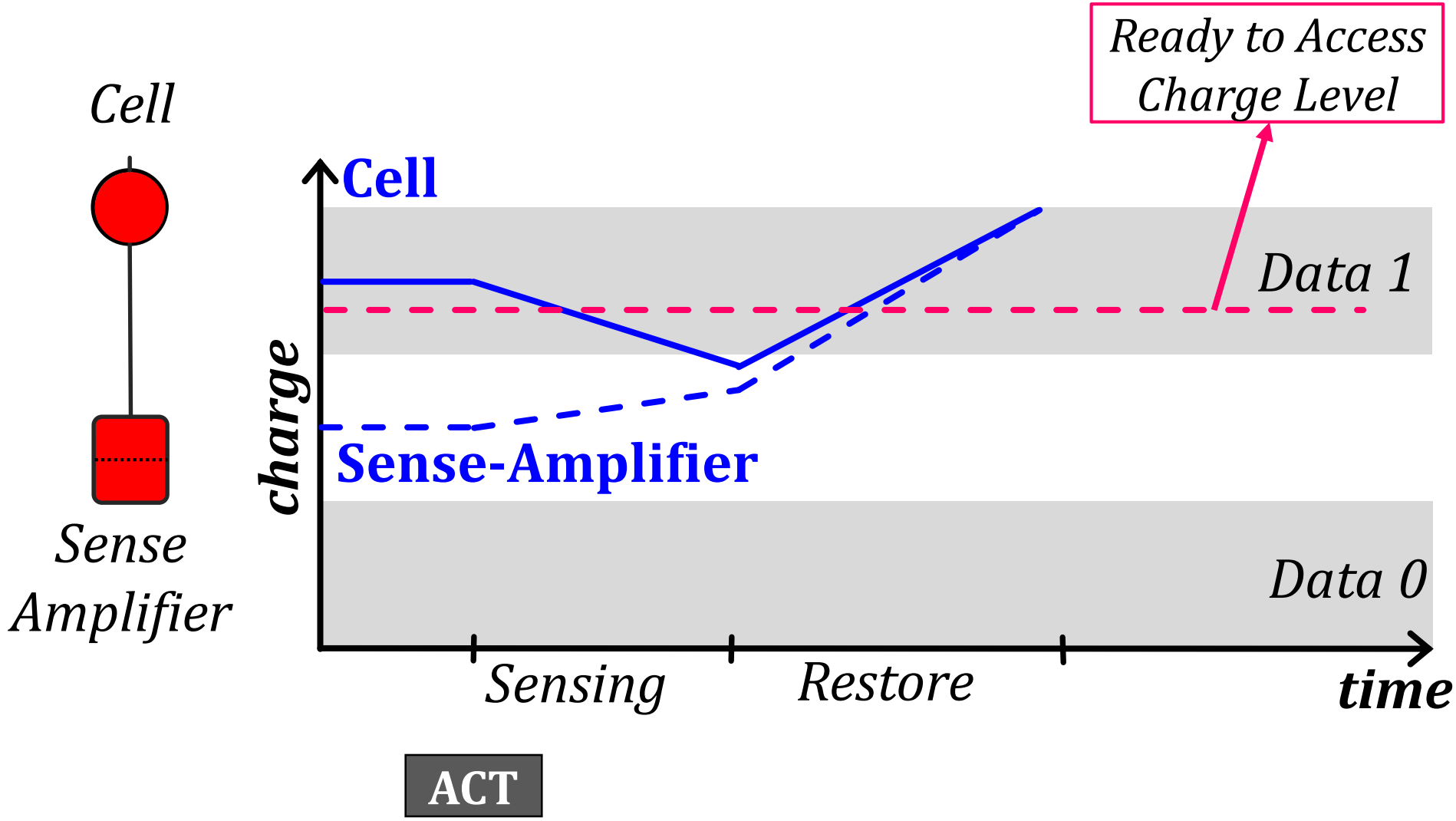
DRAM Charge over Time



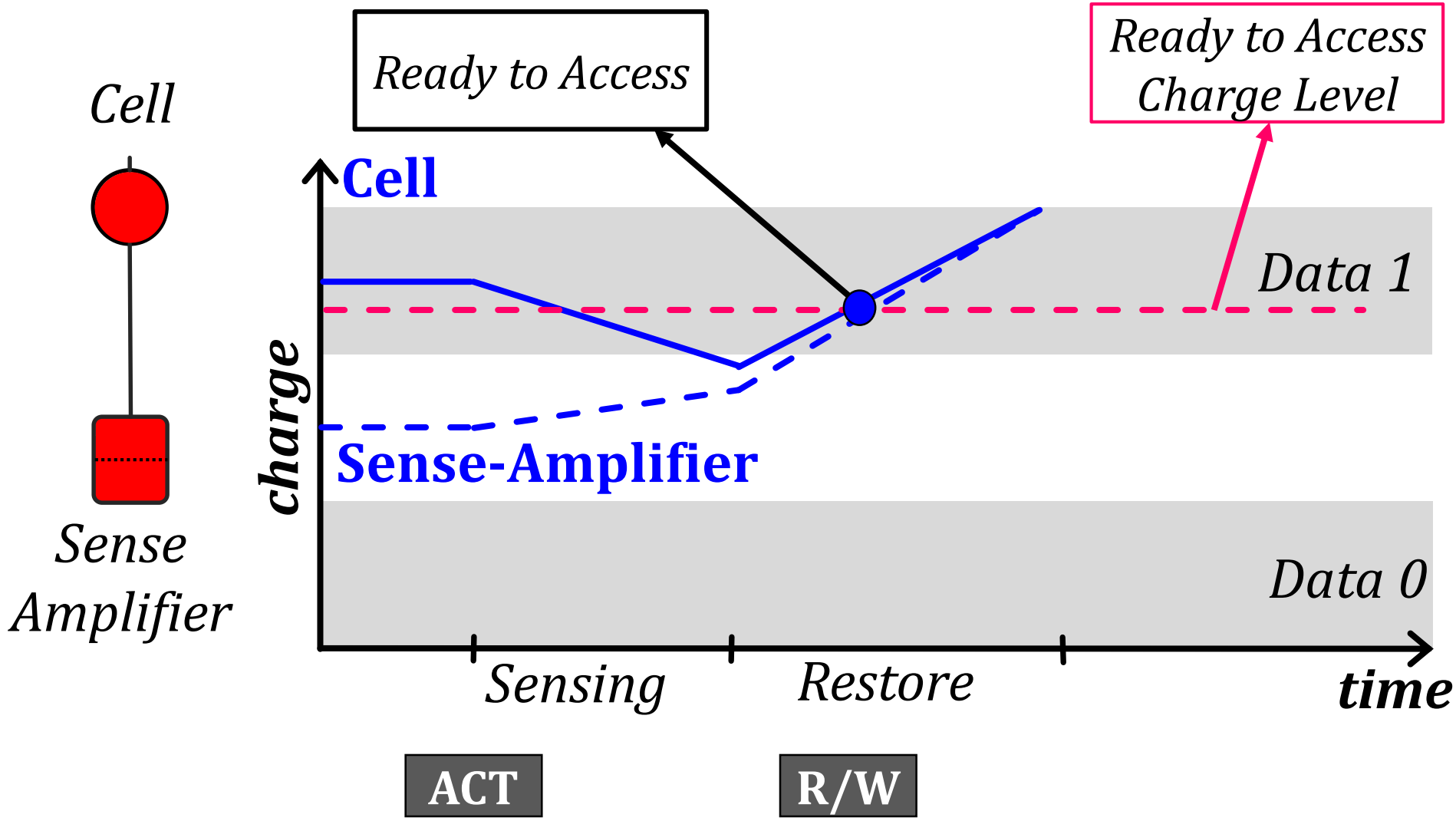
DRAM Charge over Time



DRAM Charge over Time



DRAM Charge over Time



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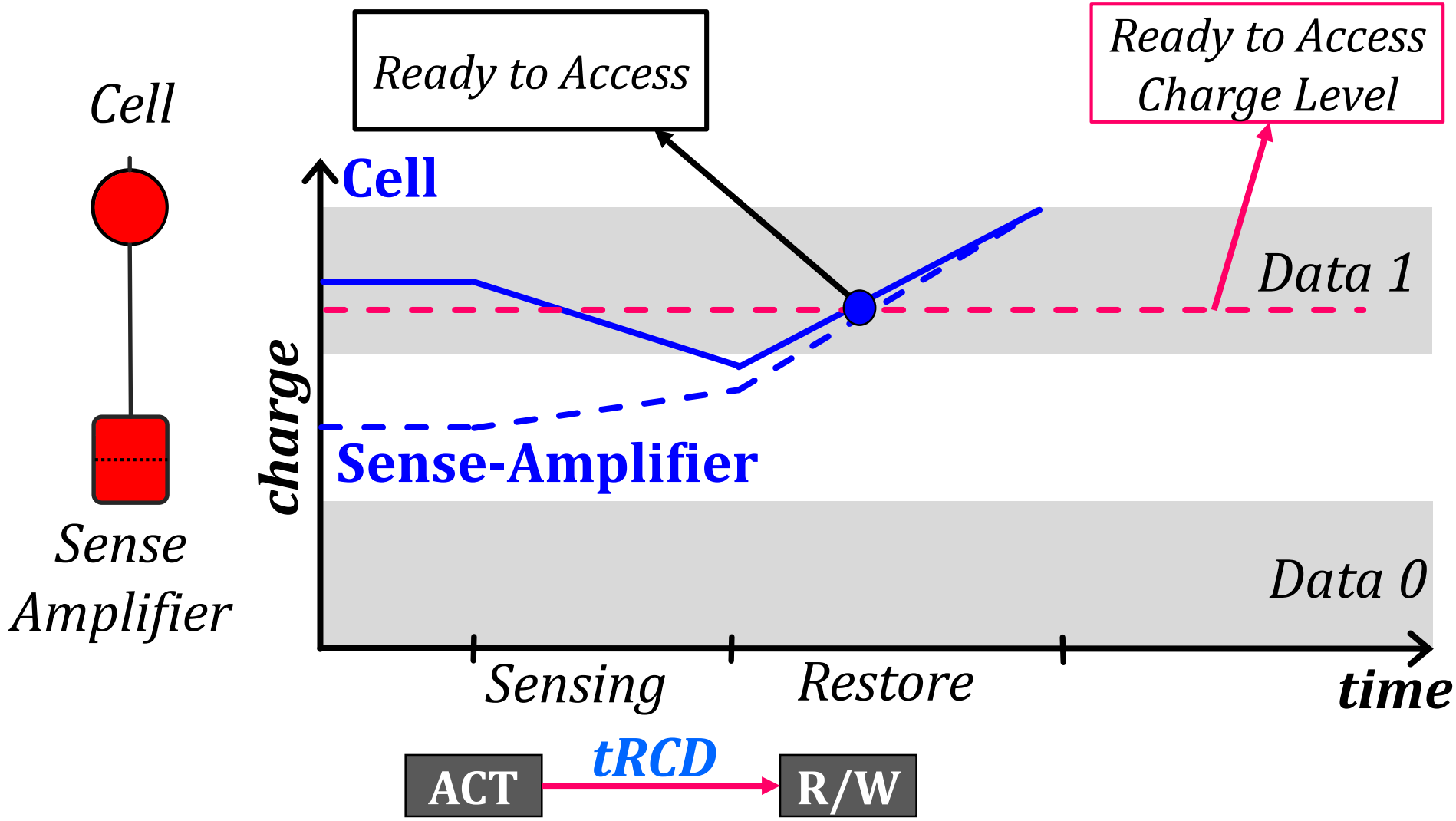
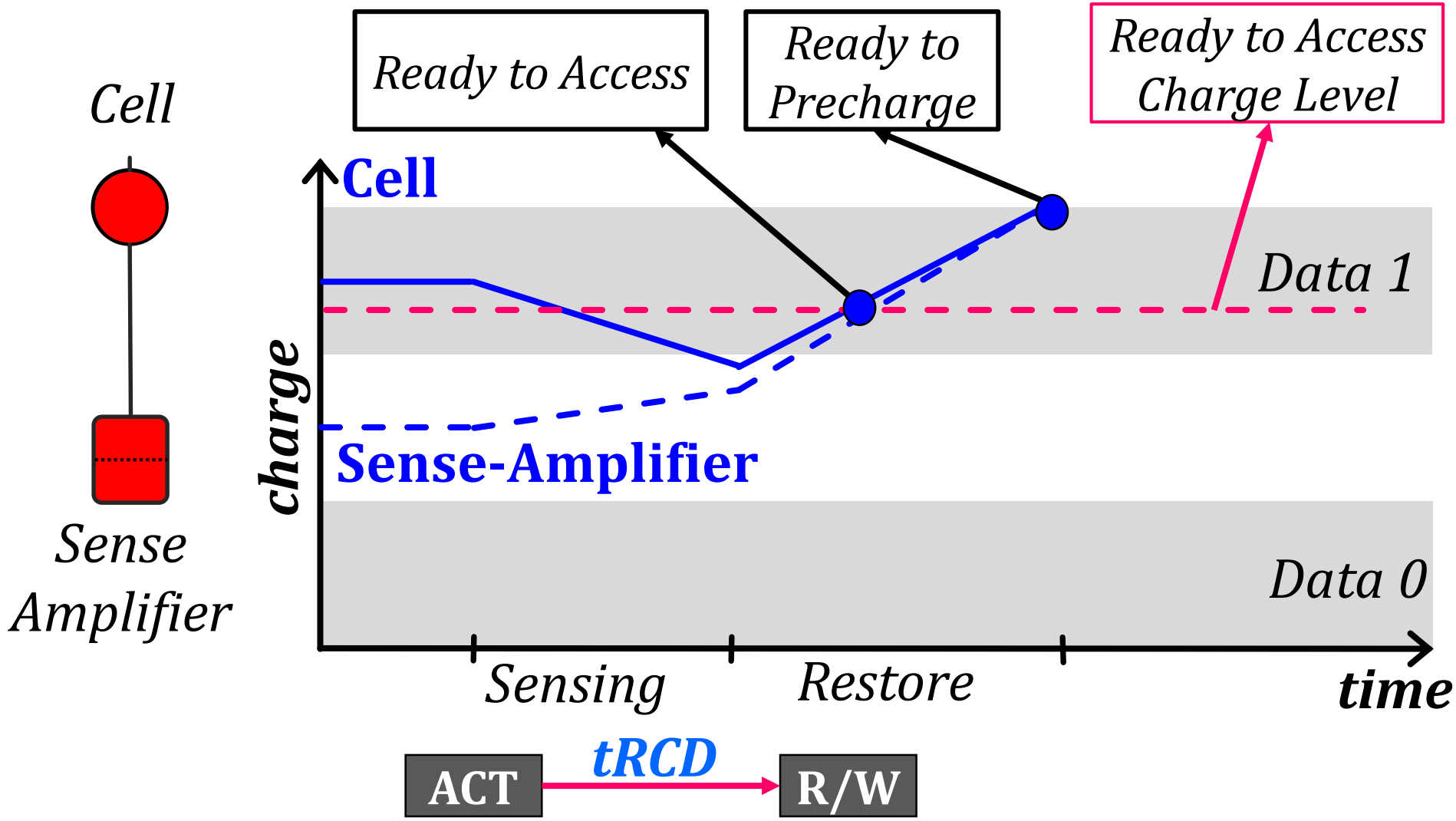
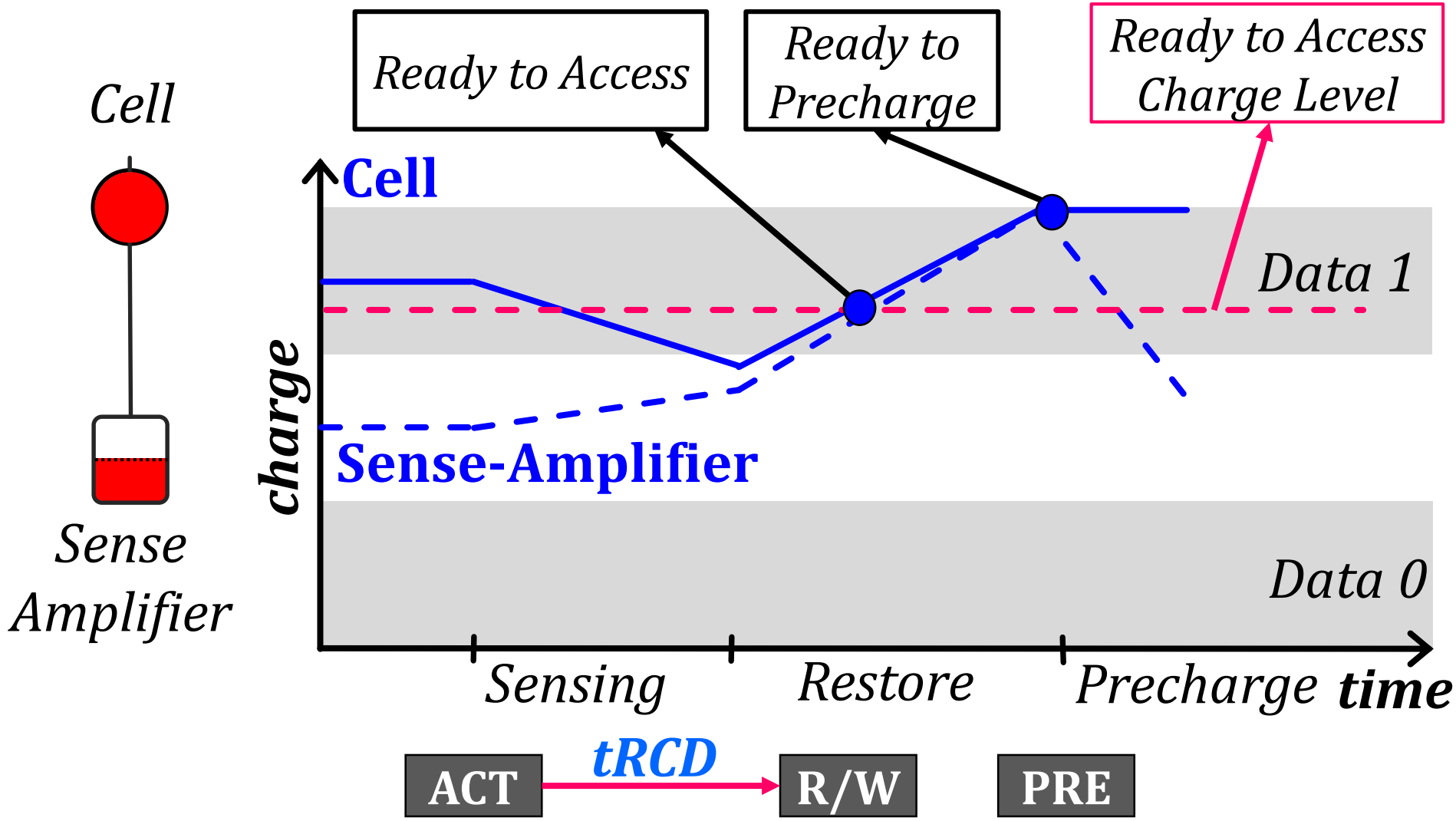


DRAM Charge over Time



DRAM Charge over Time



DRAM Charge over Time