

# **CS 211: Intro to Computer Architecture**

## ***12.1: Single-Cycle RV64I CPU - Arithmetic/Logic***

**Minesh Patel**

Spring 2025 – Tuesday 15 April

# Announcements

- Ongoing
  - **WA8:** due **Friday (April 18) @ 11:59 pm**
  - **PA4:** due **Friday (April 18) @ 11:59 pm**
- Upcoming
  - **PA5:** TBA: planned for Friday
  - **WA9:** TBA: planned for Friday

# PA6 and WA11

- Turns out both are too ambitious
- We will reweight their percentages

- **Programming Assignments (53%):** We will have 6 programming assignments weighted as follows.

**5%** ~~• [3%] PA1: Intro to Linux~~

**12%** ~~• [10%] PA2: C Development + Integers~~

**12%** ~~• [10%] PA3: Pointers, Arrays, Strings, Structs and Explicit Memory Management~~

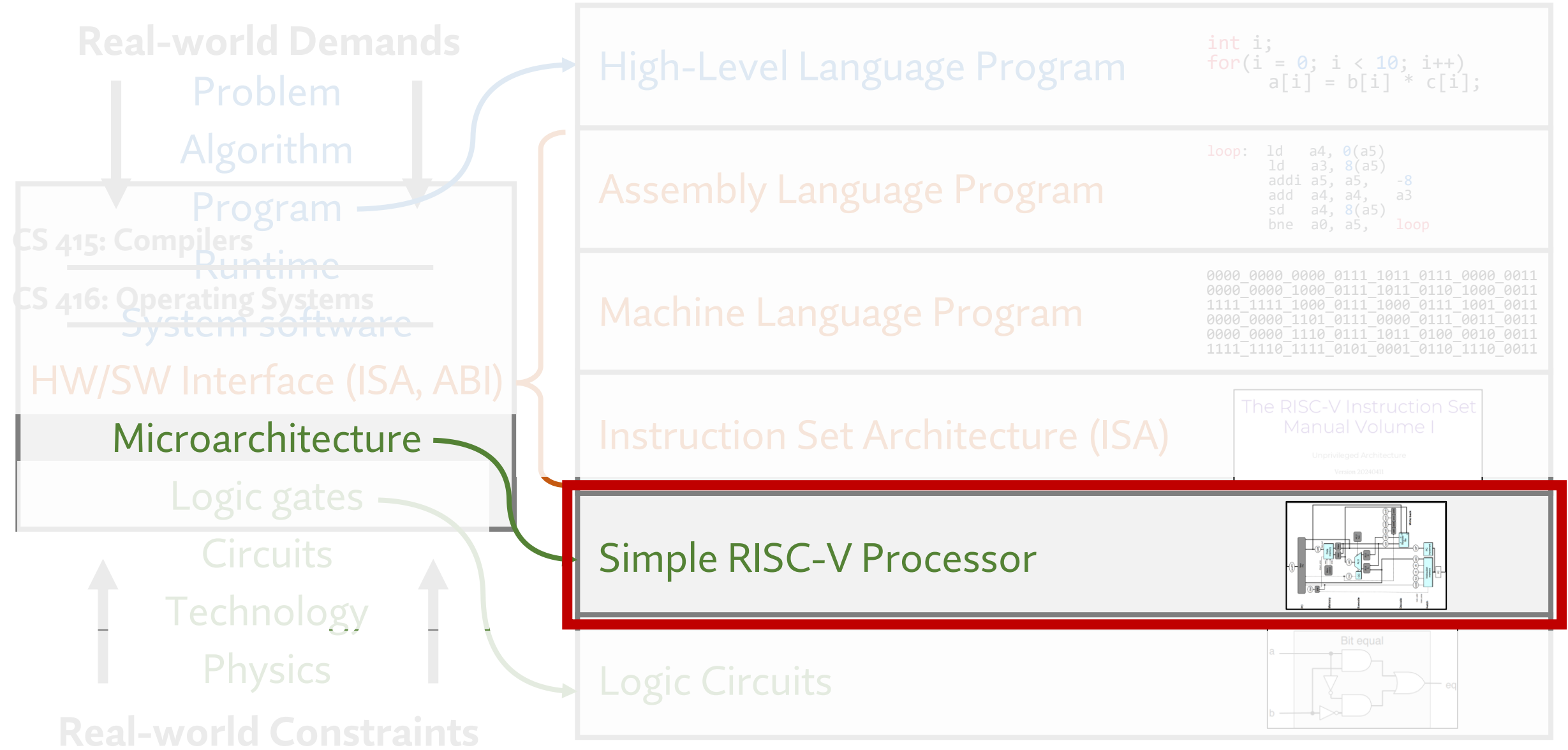
**12%** ~~• [10%] PA4: Assembly Programming~~

**12%** ~~• [10%] PA5: Single-cycle CPU Emulation~~

~~• [10%] PA6: Extension with Memory + Caches~~

- WAs still worth 12% total (~1.7% each over 7 WAs + 3 dropped)

# Layers of Abstraction for CS 211



# Reference Material

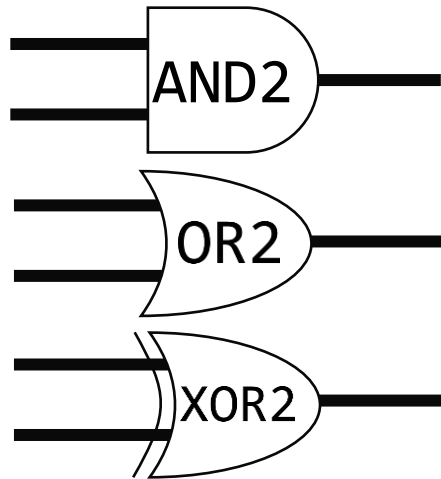
- Today's lecture partially draws inspiration from:
  - [CS 61C @ UC Berkeley](#) (Prof. Dan Garcia)

## And the RISC-V ISA Manual

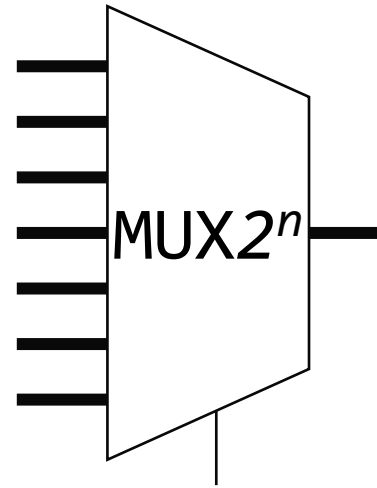
|                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Table of Contents</b>                                                 | <b>The RISC-V Instruction Set Manual Volume I:<br/>Unprivileged Architecture</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Preface</b>                                                           | <b>Version 20240411</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>1. Introduction</b>                                                   | <i>Contributors to all versions of the spec in alphabetical order (please contact editors to suggest corrections):<br/>Derek Atkins, Arvind, Krste Asanović, Rimas Avizienis, Jacob Bachmeyer, Christopher F. Batten, Allen J. Baum,<br/>Abel Bernabeu, Alex Bradbury, Scott Beamer, Hans Boehm, Preston Briggs, Christopher Celio, Chuanhua<br/>Chang, David Chisnall, Paul Clayton, Palmer Dabbelt, L. Peter Deutsch, Ken Dockser, Paul Donahue, Aaron<br/>Durbin, Roger Espasa, Greg Faver, Andy Glew, Shaked Flur, Stefan Freudenberger, Marc Gauthier, Andy Glew,<br/>Jan Gray, Gianluca Guida, Michael Hamburg, John Hauser, Christian Herber, John Ingalls, David Horner,<br/>Bruce Houl, Bill Huffman, Alexandre Joannou, Olof Johansson, Ben Keller, David Kruckemyer, Tariq Kurd,<br/>Yunsup Lee, Paul Loewenstein, Daniel Lustig, Yatin Manerkar, Luc Maranget, Ben Marshall, Margaret<br/>Martonosi, Phil McCoy, Nathan Menhorn, Christoph Müllner, Joseph Myers, Vijayanand Nagarajan, Torbjørn<br/>Viem Ness, Rishiyur Nikhil, Jonas Oberhauser, Stefan O'Rear, Markku-Juhani O. Saarinen, Albert Ou, John<br/>Ousterhout, Daniel Page, David Patterson, Christopher Pulte, Jose Renau, Josh Scheid, Colin Schmidt, Peter<br/>Sewell, Susmit Sarkar, Ved Shanbhogue, Brent Spinney, Brendan Sweeney, Michael Taylor, Wesley Terpstra,<br/>Matt Thomas, Tommy Thorn, Philipp Tomsich, Caroline Trippel, Ray VanDeWalker, Muralidaran<br/>Vijayaraghavan, Megan Wachs, Paul Wamsley, Andrew Waterman, Robert Watson, David Weaver, Derek<br/>Williams, Claire Wolf, Andrew Wright, Reinoud Zandijk, and Sizhuo Zhang.</i> |
| <b>2. RV32I Base Integer Instruction Set,<br/>Version 2.1</b>            | <i>This document is released under a Creative Commons Attribution 4.0 International License.</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>2.1. Programmers' Model for Base<br/>Integer ISA</b>                  | <i>This document is a derivative of "The RISC-V Instruction Set Manual, Volume I: User-Level ISA Version 2.1" released under the<br/>following license: ©2010-2017 Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanović. Creative Commons<br/>Attribution 4.0 International License. Please cite as: "The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Document<br/>Version 20191214-draft", Editors Andrew Waterman and Krste Asanović, RISC-V Foundation, December 2019.</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>2.2. Base Instruction Formats</b>                                     | <b>Preface</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>2.3. Immediate Encoding Variants</b>                                  | This document describes the RISC-V unprivileged architecture.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>2.4. Integer Computational<br/>Instructions</b>                       | The ISA modules marked <b>Ratified</b> have been ratified at this time. The modules marked <b>Frozen</b> are not expected to change<br>significantly before being put up for ratification. The modules marked <b>Draft</b> are expected to change before ratification.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>2.4.1. Integer Register-<br/>Immediate Instructions</b>               | The document contains the following versions of the RISC-V ISA modules:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
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| <b>2.5.2. Conditional Branches</b>                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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| <b>2.9. HINT Instructions</b>                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>3. RV32E and RV64E Base Integer<br/>Instruction Sets, Version 2.0</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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| <b>3.2. RV32E and RV64E Instruction<br/>Set Encoding</b>                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>4. RV64I Base Integer Instruction Set,<br/>Version 2.1</b>            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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| <b>4.2. Integer Computational</b>                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

# Recap: Combinational Logic Circuits

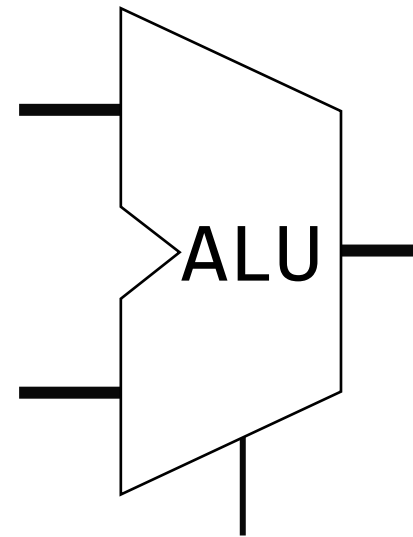
**Individual  
Logic Gates**



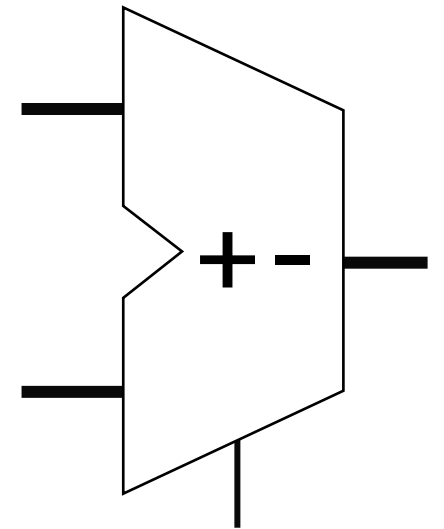
**Multiplexer**



**ALU**



**Add/Sub**



**Today:** Combine these to execute a RISC-V program

# Agenda

- **Single-Cycle CPU**
  - State Elements
- Five-Stage Execution Model
  - Implementing an ADD
  - R-TYPE Instructions
  - Any Instruction

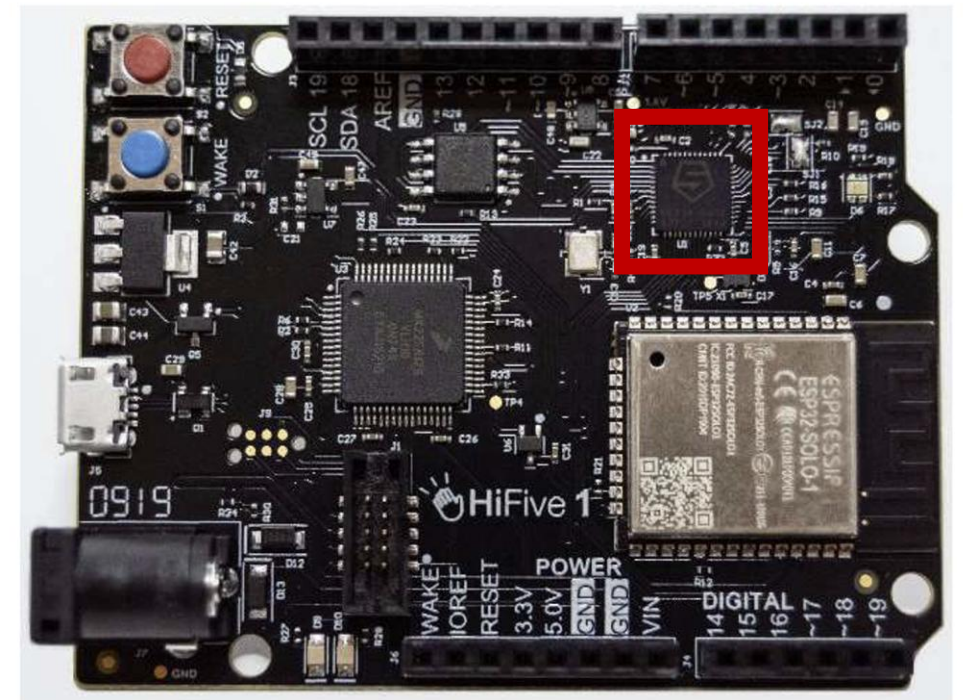
# Goal

- Design a CPU to execute all RV64I instructions

| Opcode     | Instruction             | Fmt | Example           | Description              | Notes                  |
|------------|-------------------------|-----|-------------------|--------------------------|------------------------|
| li         | load immediate          | *   | li a0, 2          | addi a0, zero, 2         | <i>pseudo</i>          |
| la         | load address            | *   | la a0, symbol     | a0 = symbol              | <i>pseudo, 2 instr</i> |
| add        | add                     | R   | add a0, a1, a2    | a0 = a1 + a2             | sign-extends           |
| sub        | subtract                | R   | sub a0, a1, a2    | a0 = a1 - a2             |                        |
| xor        | bitwise exclusive or    | R   | xor a0, a1, a2    | a0 = a1 ^ a2             |                        |
| or         | bitwise or              | R   | or a0, a1, a2     | a0 = a1   a2             |                        |
| and        | bitwise and             | R   | and a0, a1, a2    | a0 = a1 & a2             |                        |
| sll        | shift left logical      | R   | sll a0, a1, a2    | a0 = a1 << a2            |                        |
| srl        | shift right logical     | R   | srl a0, a1, a2    | a0 = a1 >> a2            |                        |
| sra        | shift right arith*      | R   | sra a0, a1, a2    | a0 = a1 >> a2            |                        |
| slt        | set less than           | R   | slt a0, a1, a2    | a0 = (a1 < a2) ? 1 : 0   | unsigned               |
| sltu       | set less than (u)       | R   | sltu a0, a1, a2   | a0 = (a1 < a2) ? 1 : 0   |                        |
| addi       | add immediate           | I   | addi a0, a1, 2    | a0 = a1 + 2              | sign-extends           |
| xori       | xor immediate           | I   | xori a0, a1, 2    | a0 = a1 ^ 2              |                        |
| ori        | or immediate            | I   | ori a0, a1, 2     | a0 = a1   2              |                        |
| andi       | and immediate           | I   | andi a0, a1, 2    | a0 = a1 & 2              |                        |
| slli       | shift left logical imm  | I   | slli a0, a1, 2    | a0 = a1 << 2             |                        |
| srl        | shift right logical imm | I   | srl a0, a1, 2     | a0 = a1 >> 2             |                        |
| srai       | shift right arith imm   | I   | srai a0, a1, 2    | a0 = a1 >> 2             |                        |
| slti       | set less than imm       | I   | slti a0, a1, 2    | a0 = (a1 < 2) ? 1 : 0    |                        |
| sltiu      | set less than imm (u)   | I   | sltiu a0, a1, 2   | a0 = (a1 < 2) ? 1 : 0    | unsigned               |
| mv         | move (copy)             | *   | mv a0, a1         | addi a0, a1, 0           | <i>pseudo</i>          |
| neg        | 2s-complement negation  | *   | neg a0, a1        | sub a0, zero, a1         | <i>pseudo</i>          |
| not        | bitwise not             | *   | not a0, a1        | xori a0, a1, -1          | <i>pseudo</i>          |
| lb         | load byte               | I   | lb a0, 1(a1)      | a0 = M[a1+1] (8 bits)    | zero-extends           |
| lh         | load half               | I   | lh a0, 2(a1)      | a0 = M[a1+2] (16 bits)   |                        |
| lw         | load word               | I   | lw a0, 4(a1)      | a0 = M[a1+4] (32 bits)   |                        |
| ld         | load double word        | I   | ld a0, 8(a1)      | a0 = M[a1+8] (64 bits)   |                        |
| lbu        | load byte (u)           | I   | lbu a0, 1(a1)     | a0 = M[a1+1] (8 bits)    |                        |
| lhu        | load half (u)           | I   | lhu a0, 2(a1)     | a0 = M[a1+2] (16 bits)   |                        |
| lwu        | load word (u)           | I   | lwu a0, 4(a1)     | a0 = M[a1+4] (32 bits)   |                        |
| l{b h w d} | load global             | *   | ld a0, symbol     | a0 = M[symbol]           | <i>pseudo, 2 instr</i> |
| sb         | store byte              | S   | sb a0, 1(a1)      | M[a1+1] = a0 (8 bits)    | <i>pseudo, 2 instr</i> |
| sh         | store half              | S   | sh a0, 2(a1)      | M[a1+2] = a0 (16 bits)   |                        |
| sw         | store word              | S   | sw a0, 4(a1)      | M[a1+4] = a0 (32 bits)   |                        |
| sd         | store double word       | S   | sd a0, 8(a1)      | M[a1+8] = a0 (64 bits)   |                        |
| s{b h w d} | store global            | *   | sd a0, symbol, t0 | M[symbol] = a0 (uses t0) |                        |
| breq       | branch if =             | B   | breq a0, a1, 2b   | if (a0 == a1) goto 2b    |                        |
| bne        | branch if ≠             | B   | bne a0, a1, 2f    | if (a0 != a1) goto 2f    |                        |



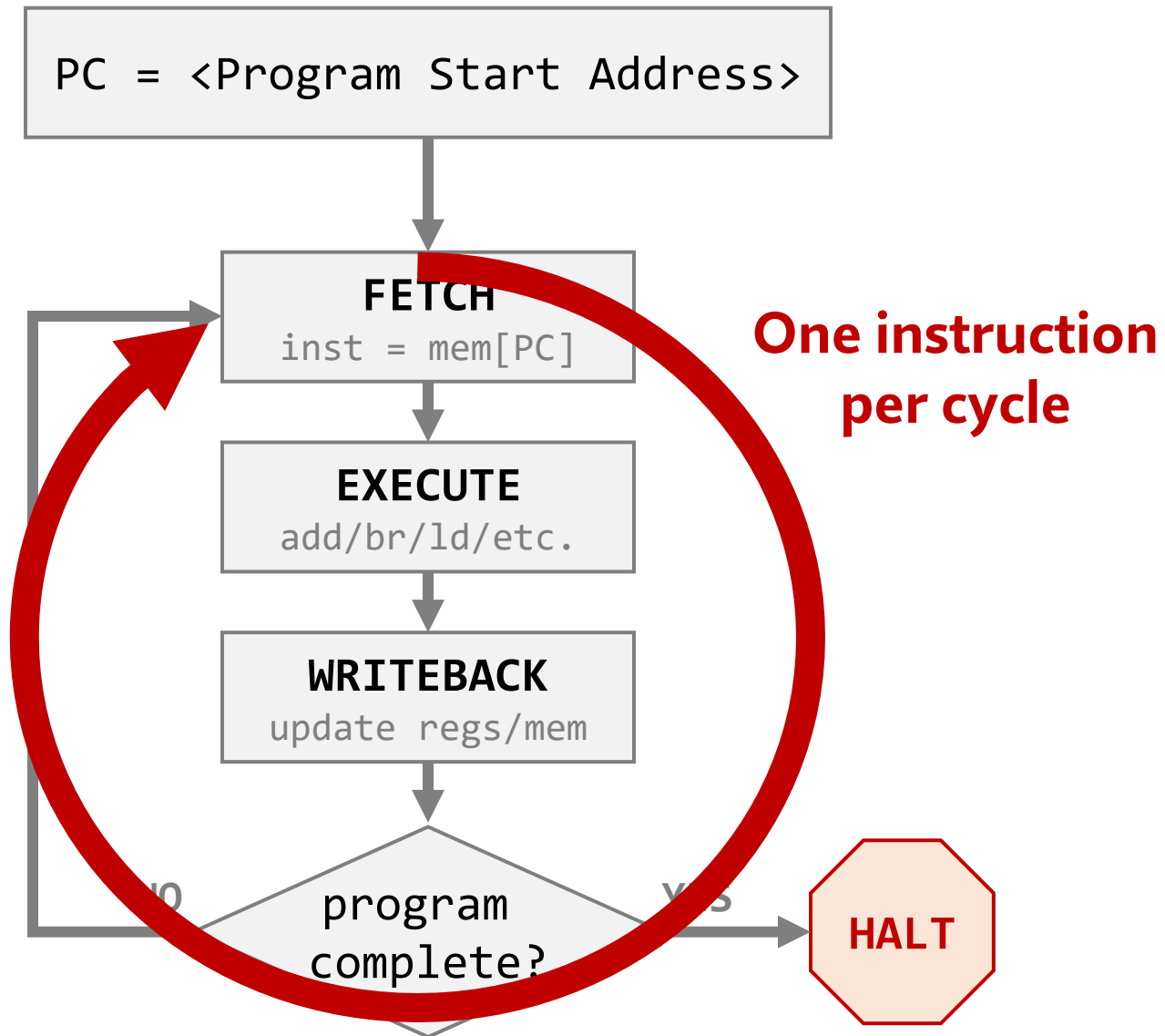
 **HiFive 1 Rev B01**



<https://www.cs.utah.edu/cs/2810/riscv-card.pdf>

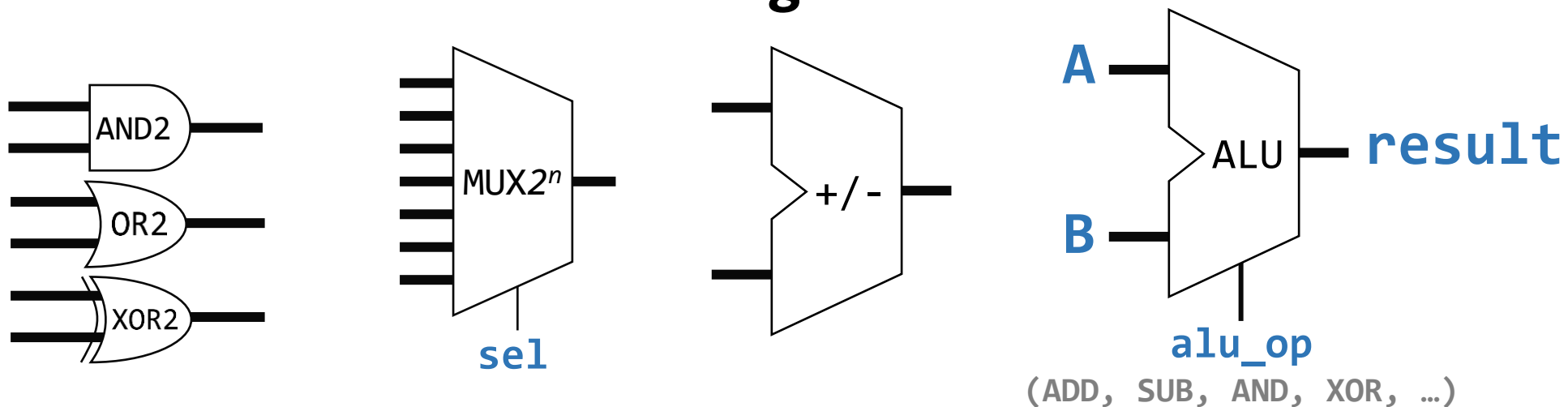
SiFive, “HiFive1 Rev B Schematics,” 2021.

# General CPU Control Flow

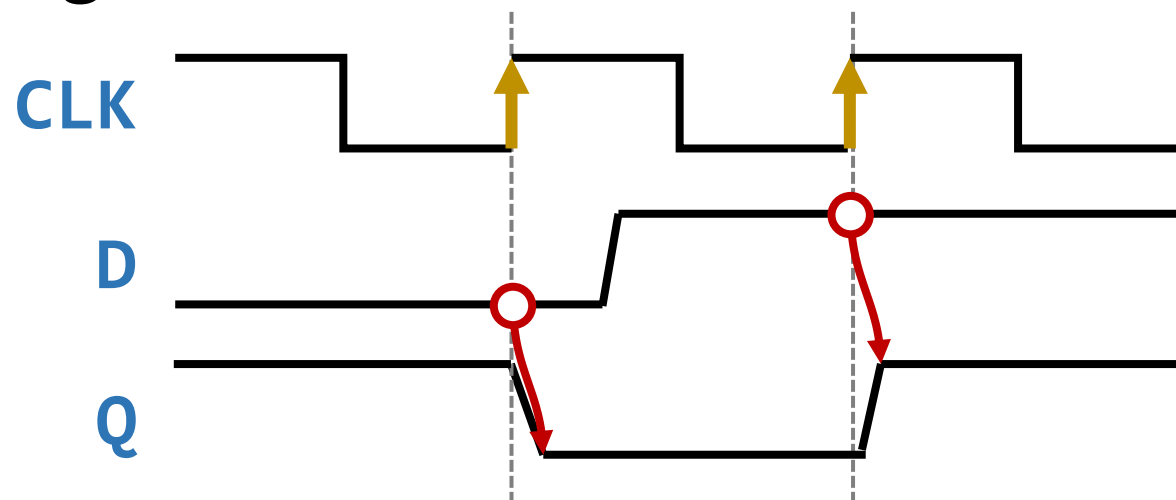
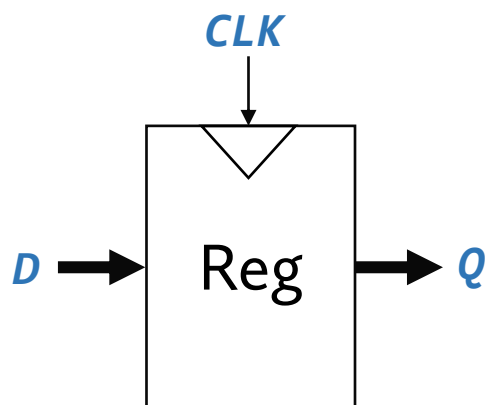


# Our Building Blocks

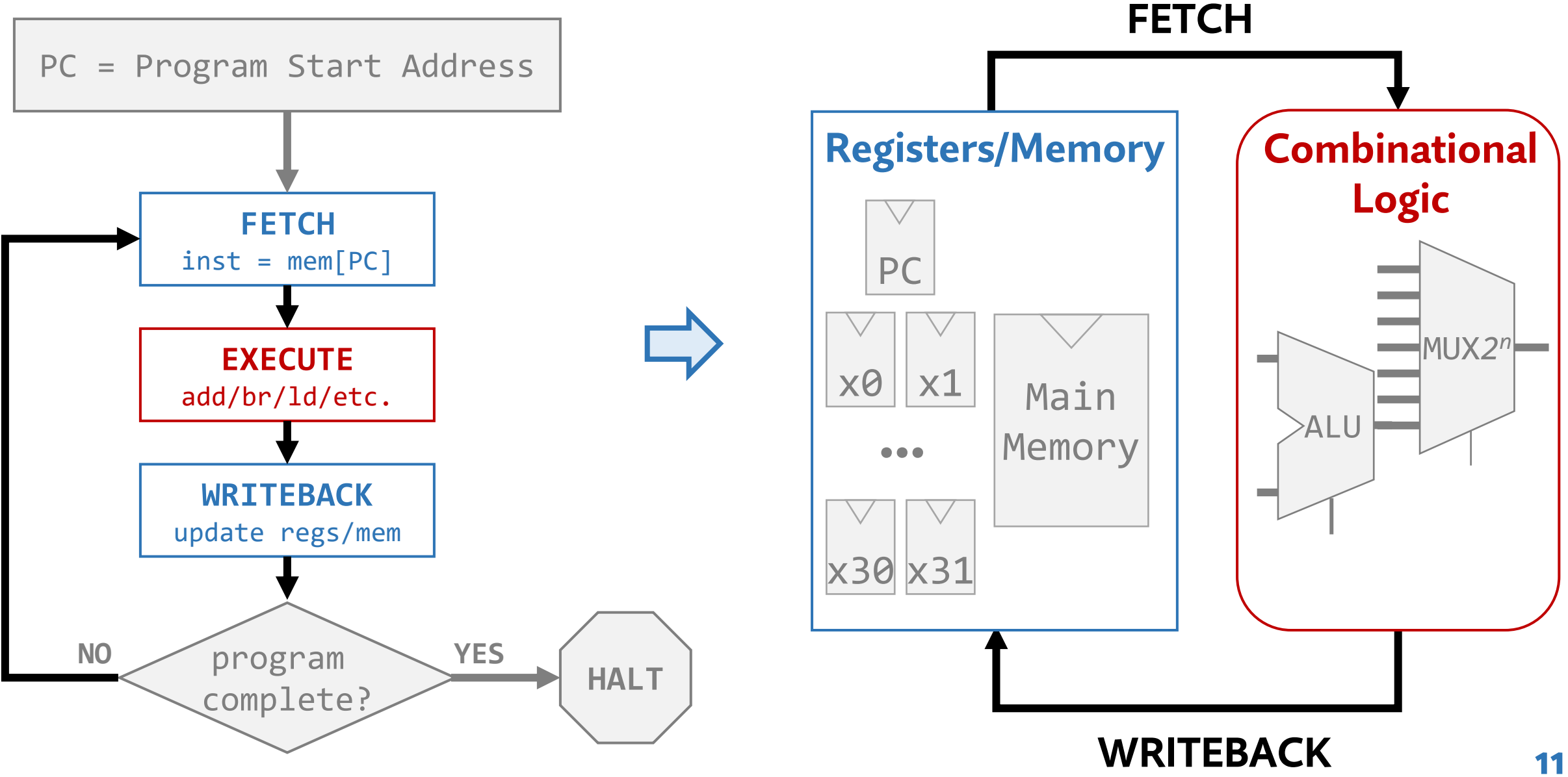
## Combinational Logic Blocks



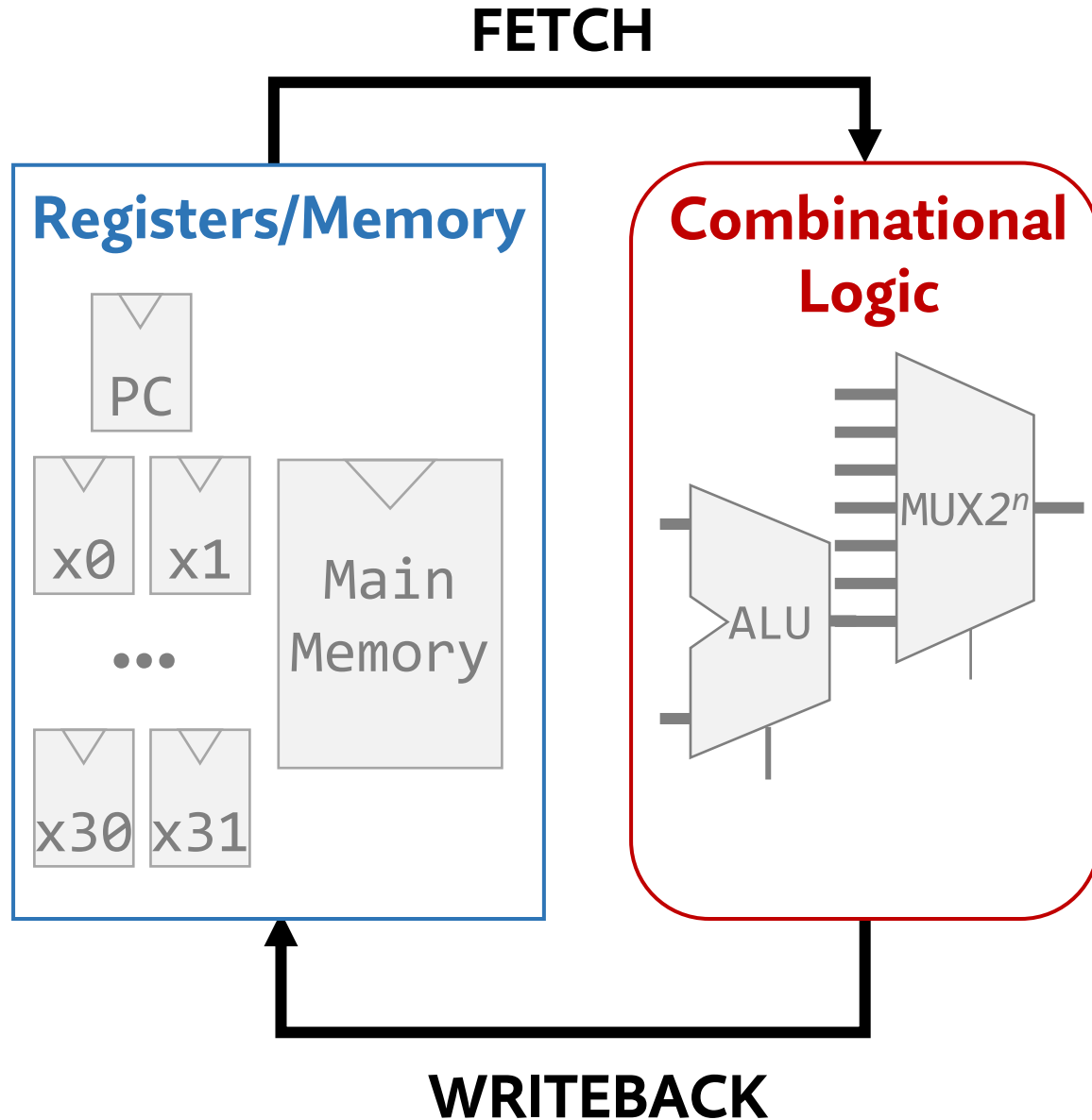
## Registers



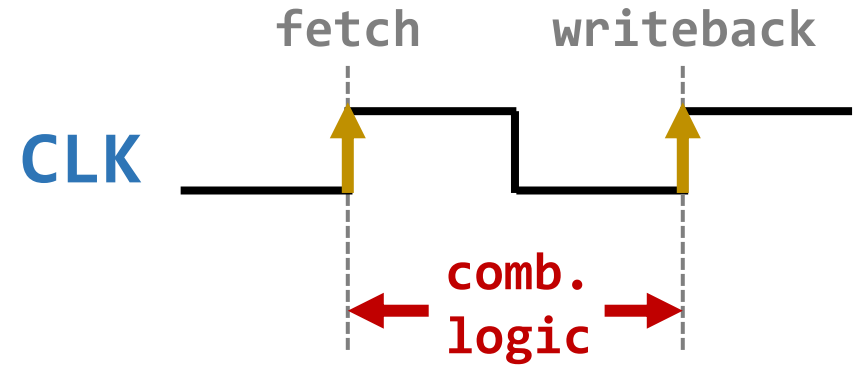
# From Abstraction to Logic Circuits



# One Instruction Per Clock Cycle



Executes **any** RV64I instruction within **one clock cycle**



$$freq = \frac{1}{cycle\ time}$$

**Example:** 4 GHz = 4 billion cycles/second  
**Cycle time:** 0.25 ns

# 4 Billion Instructions per Second

- How long would it take for you to calculate **four billion** 64-bit ADDs?

## Pen + Paper

$$4 \text{ billion adds} \times \frac{60 \text{ seconds}}{\text{add}} \times \frac{1 \text{ hour}}{3600 \text{ seconds}} \times \frac{1 \text{ year}}{8760 \text{ hours}} = 7610.35 \text{ years}$$

## 4 GHz Single-Cycle CPU

**1 second\***

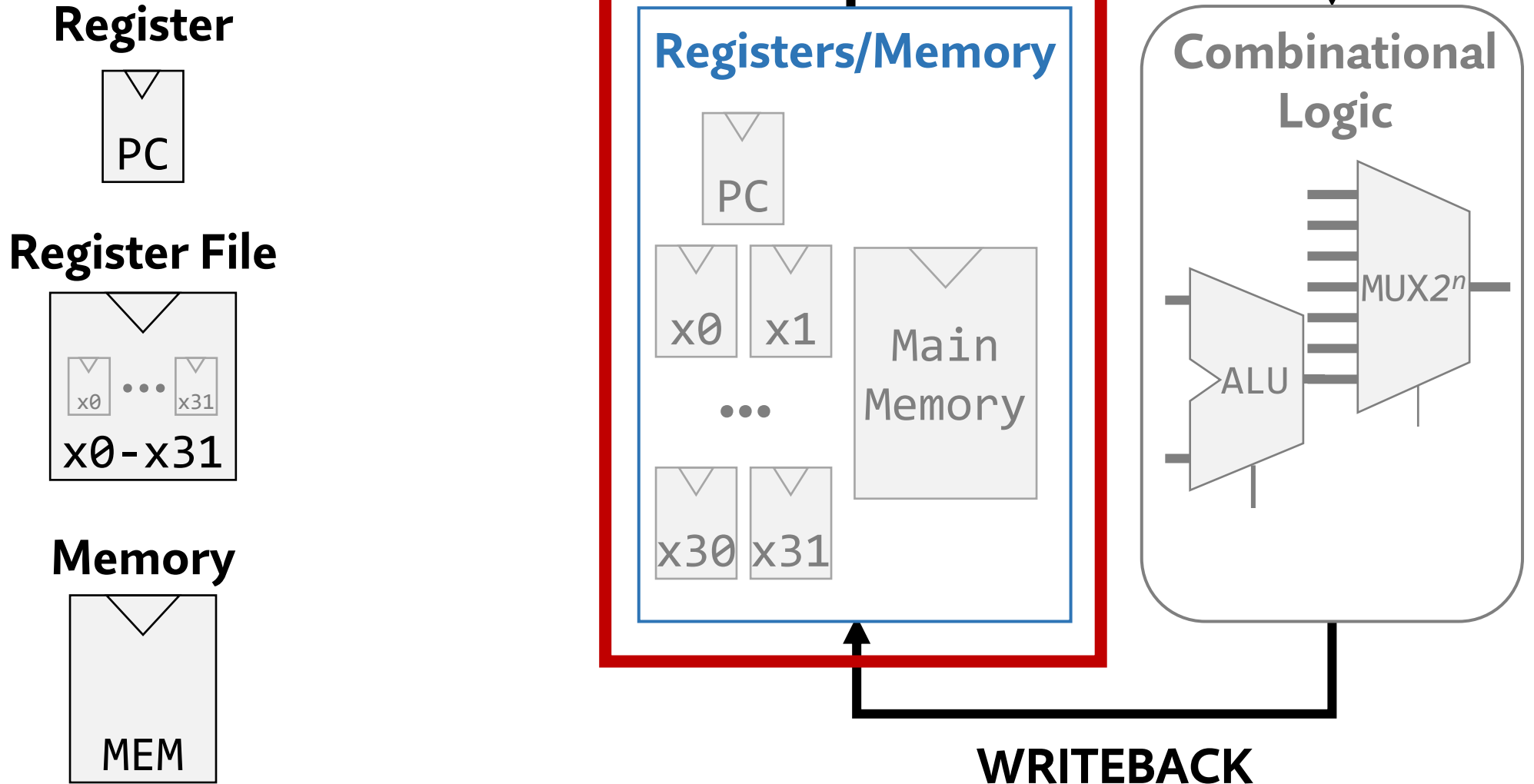
*\*lots of assumptions (e.g., no memory accesses)*

# Agenda

- Single-Cycle CPU
  - **State Elements**
- Five-Stage Execution Model
  - Implementing an ADD
  - R-TYPE Instructions
  - Any Instruction

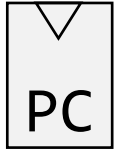
# Three State Elements

- Instructions modify the system state

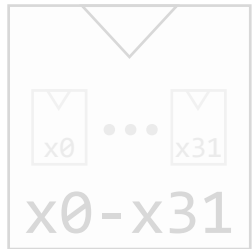


# State Element 1/3: Program Counter

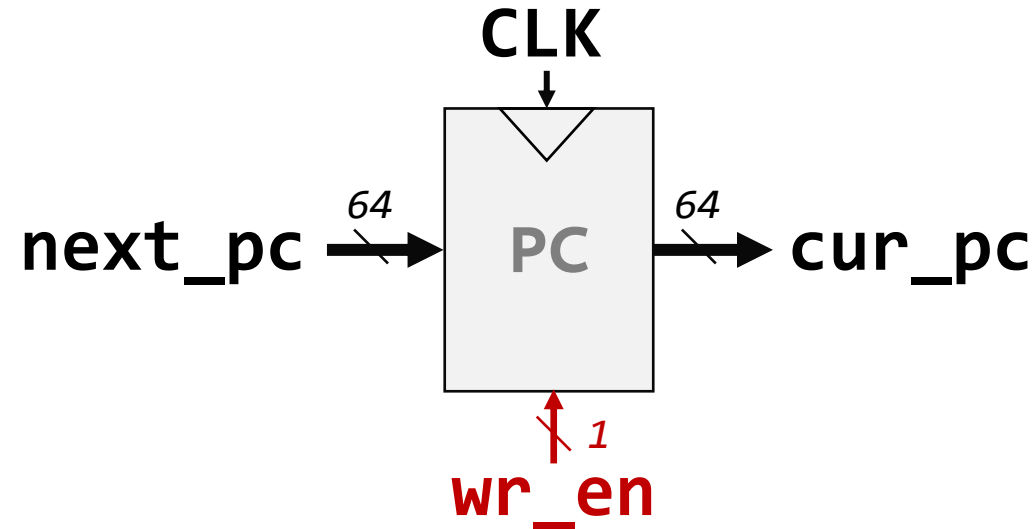
Register



Register File



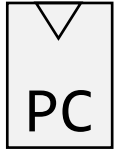
Memory



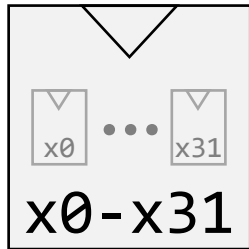
- **cur\_pc** is stable **throughout** the clock cycle
- **if(wr\_en)**  
    **cur\_pc** becomes **next\_pc** at the **end of the cycle**

# State Element 2/3: Register File

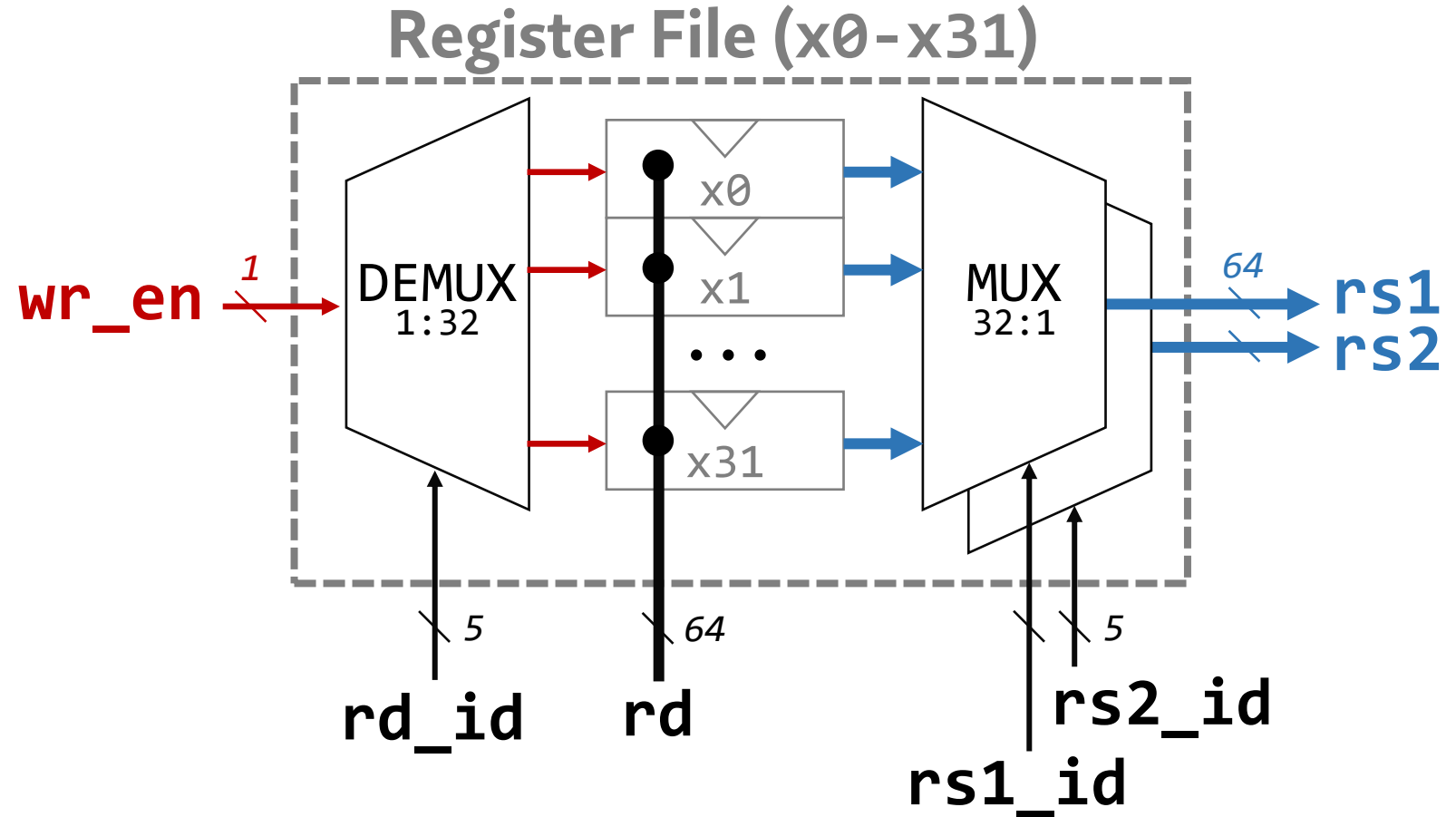
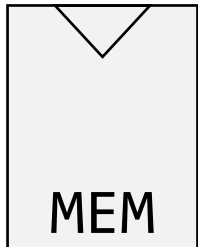
## Register



## Register File

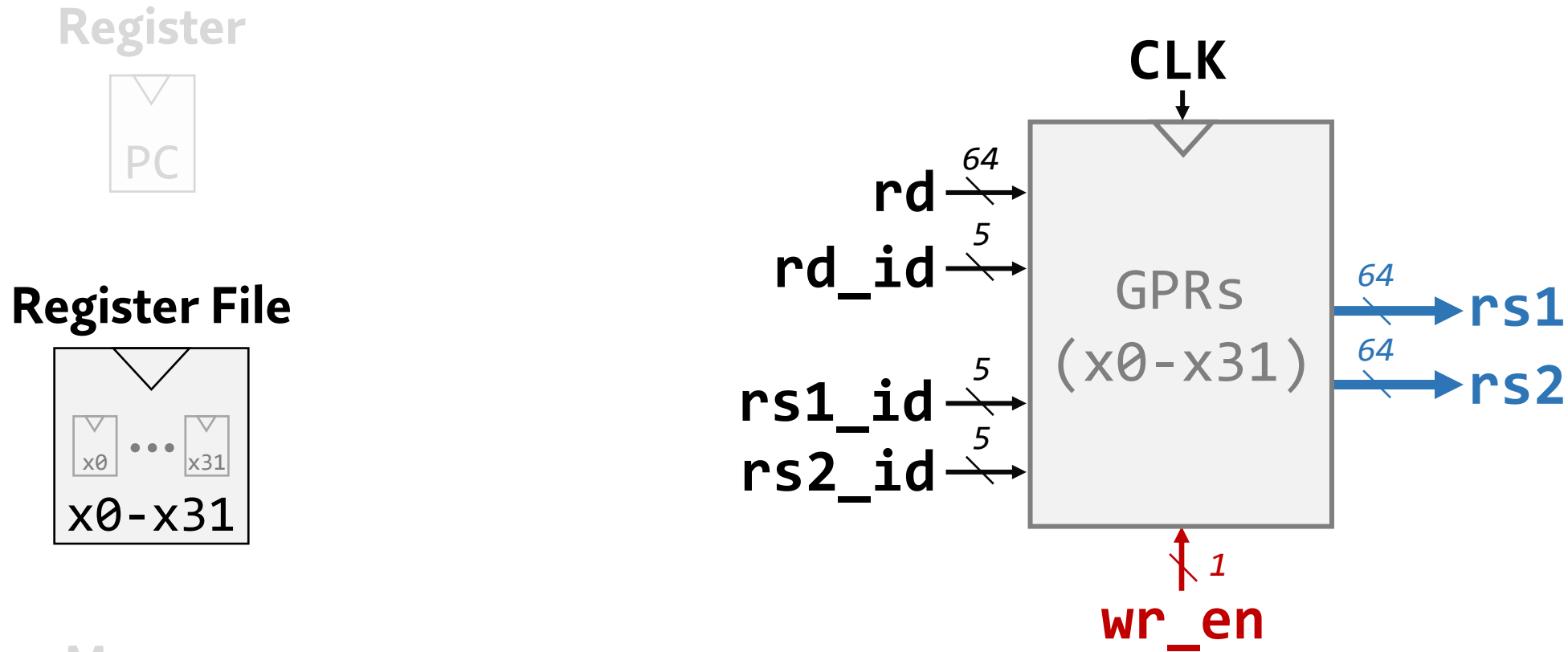


## Memory



- Combines 32 registers into one logic block
  - **rd**: one write input
  - **rs1/rs2**: two read outputs

# State Element 2/3: Register File (Abstract)



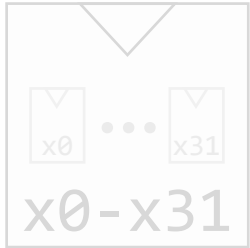
- Combines 32 registers into one logic block
  - **rd**: one write input
  - **rs1/rs2**: two read outputs

# State Element 3/3: Main Memory

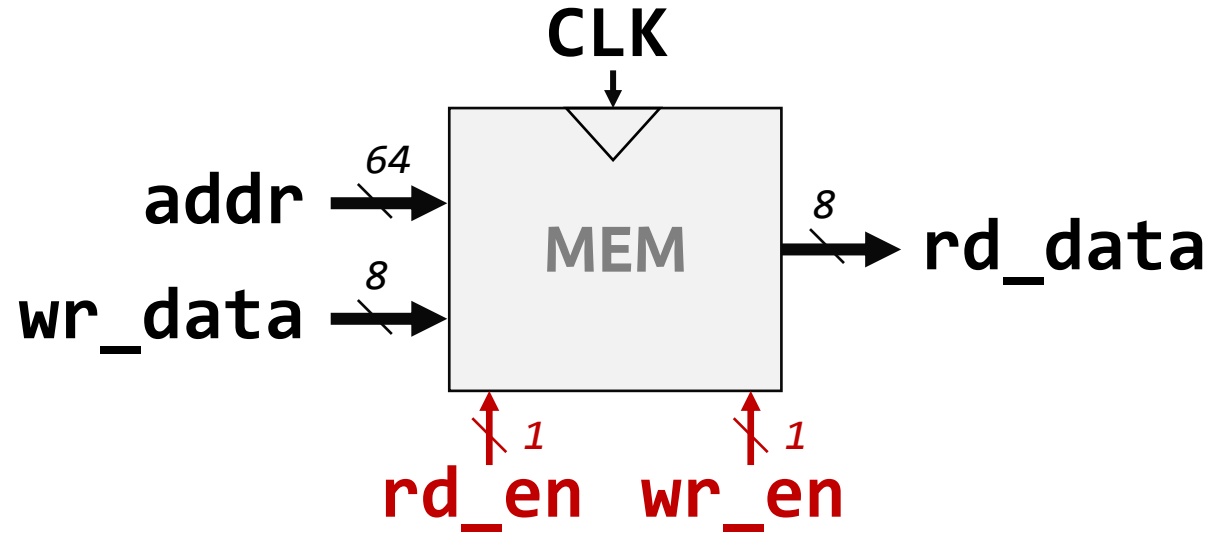
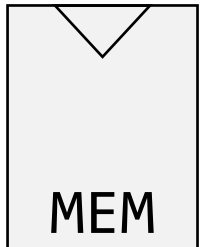
Register



Register File



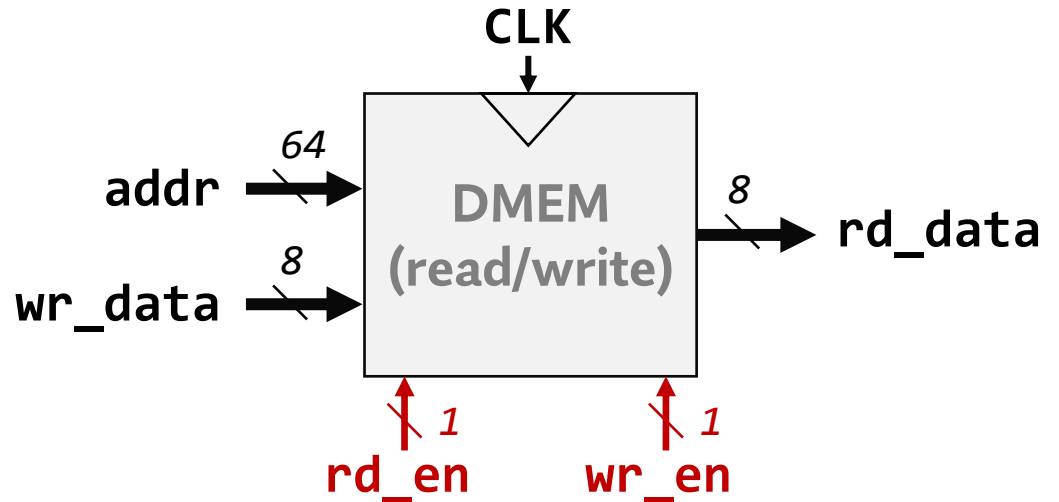
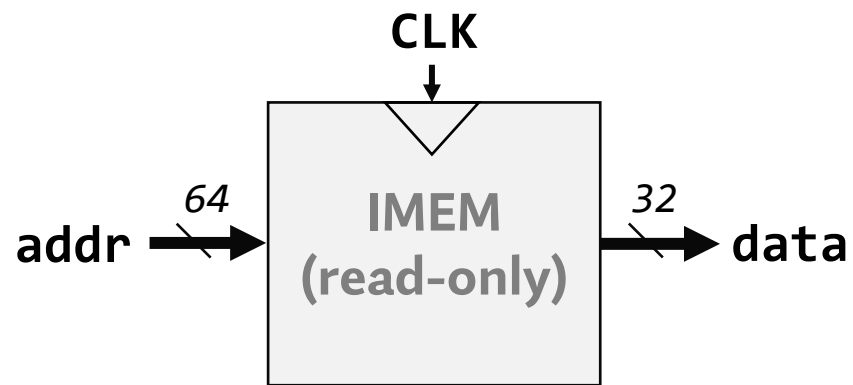
Memory



- Memory is “**magic**”
- Assume:
  - Byte addressable (8-bit read/write interface)
  - 64-bit address ( $2^{64}$  unique byte locations)

# “Two” Memories: Instructions and Data

- We draw main memory as split into two parts (**just notation!**)



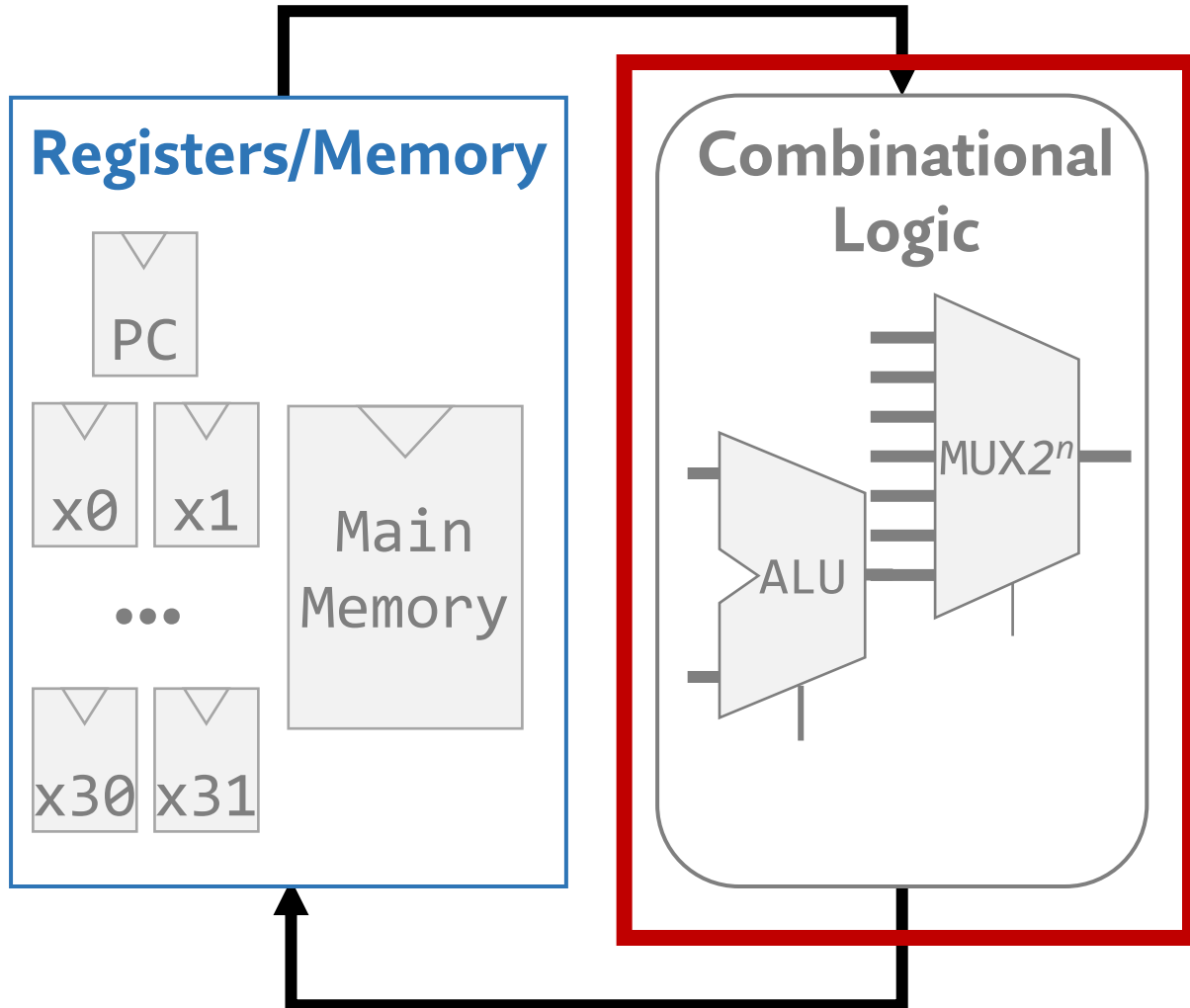
- There's still only one **actual main memory**
  - IMEM/DMEM are placeholders for **caches** (more on that later)

# Agenda

- Single-Cycle CPU
  - State Elements
- **Five-Stage Execution Model**
  - Implementing an ADD
  - R-TYPE Instructions
  - Any Instruction

# Implementing the Combinational Logic

FETCH

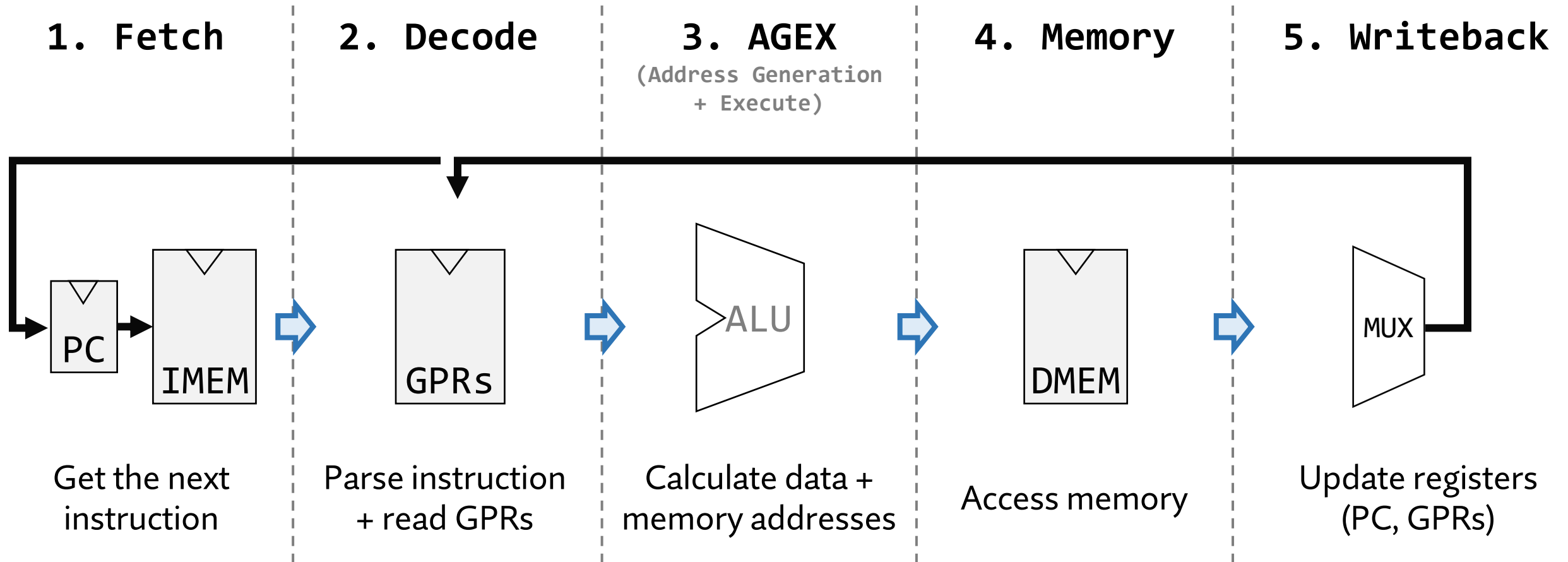


**Problem:** hard to design and build as one giant blob

**Solution:** split it into smaller “stages” and connect them together

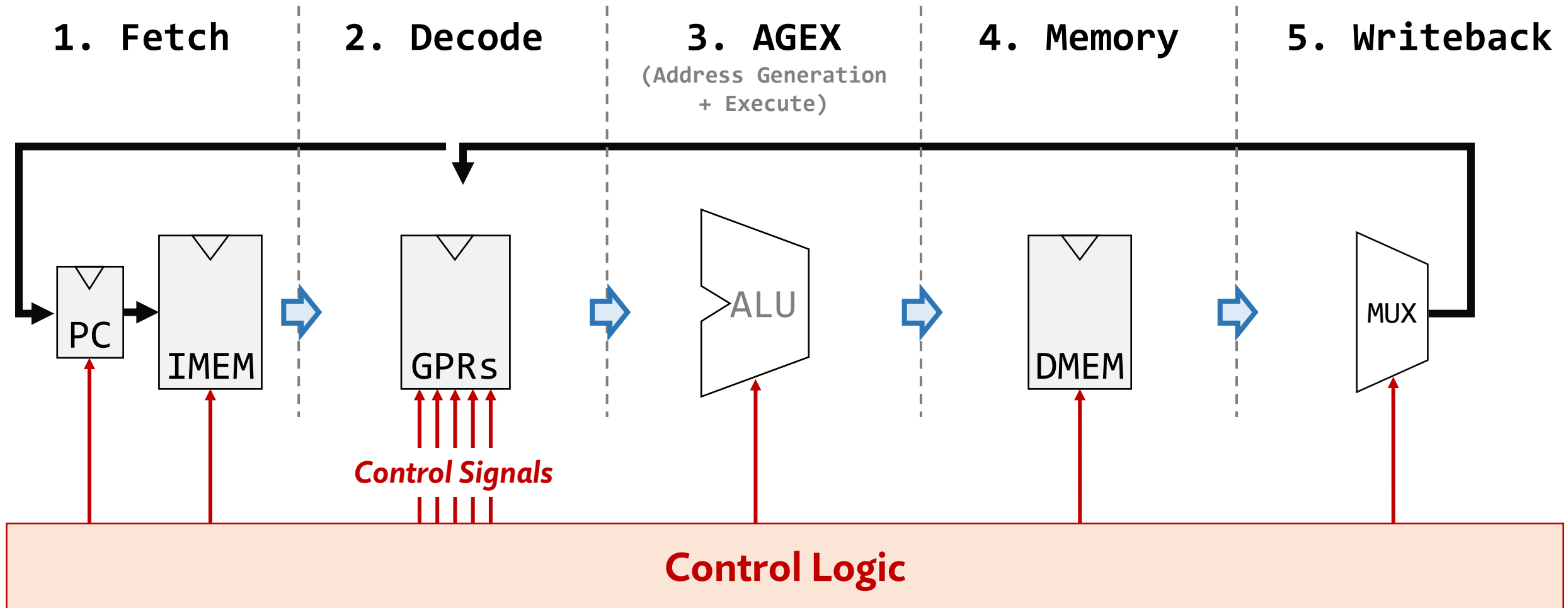
WRITEBACK

# Five-Stage CPU: Datapath



**Datapath:** Should have everything we need to execute any instruction

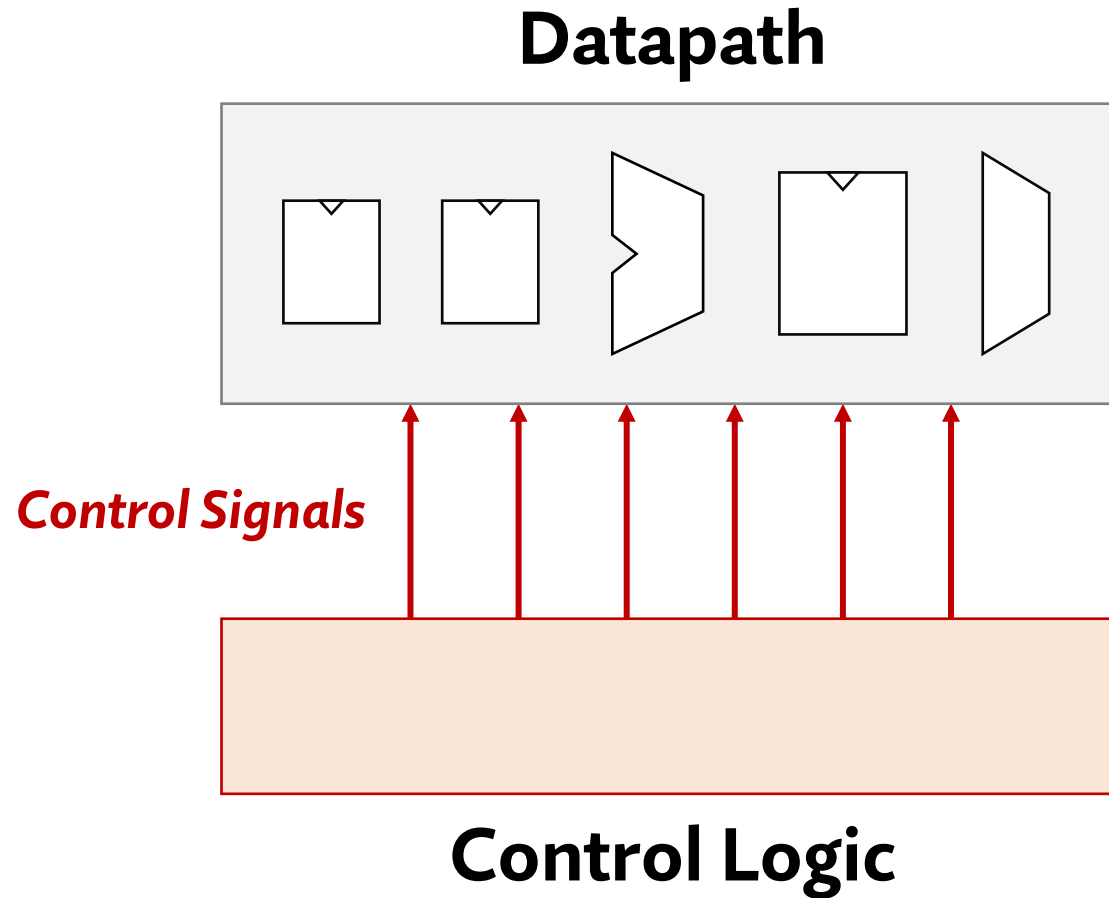
# Five-Stage CPU: Control Logic



- Control logic decides what to do **for a specific instruction** (e.g., add)

# Summary: General CPU Architecture

- **Datapath** provides logic to perform *any* RISC-V operation



- **Control logic** orchestrates the datapath for a given instruction

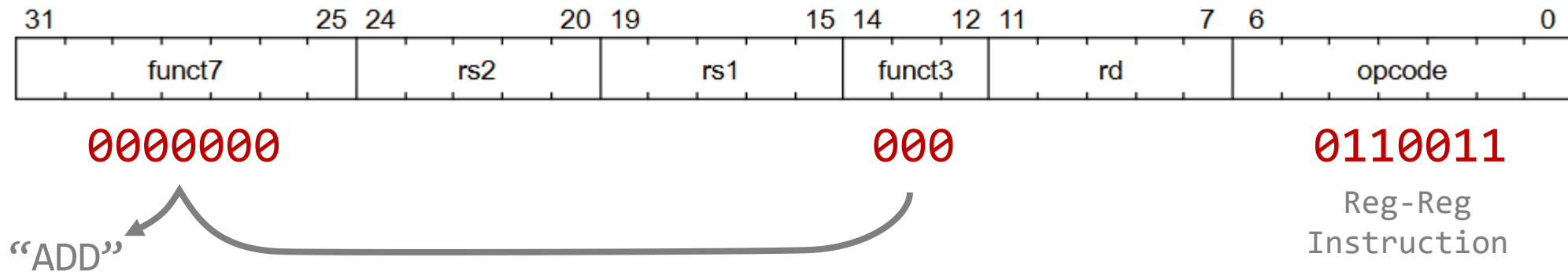
# Agenda

- Single-Cycle CPU
  - State Elements
- Five-Stage Execution Model
  - **Implementing an ADD**
  - R-TYPE Instructions
  - Any Instruction

# Starting with an add

- **Approach:** start simple

`add rd, rs1, rs2`

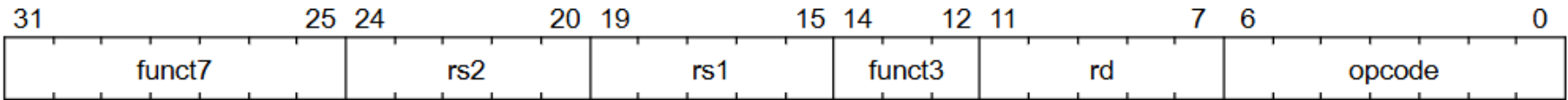
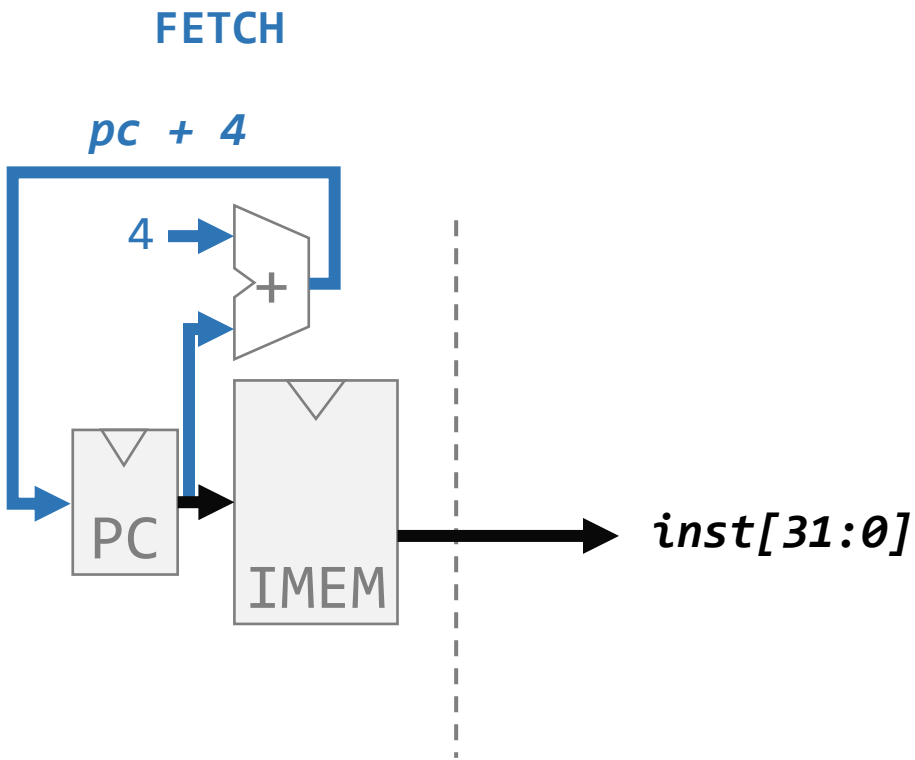


| State Element | Action                    |
|---------------|---------------------------|
| PC            | PC += 4                   |
| GPRs          | $R[rd] = R[rs1] + R[rs2]$ |
| DMEM          | -                         |

Just need the **control signals** that make all this happen

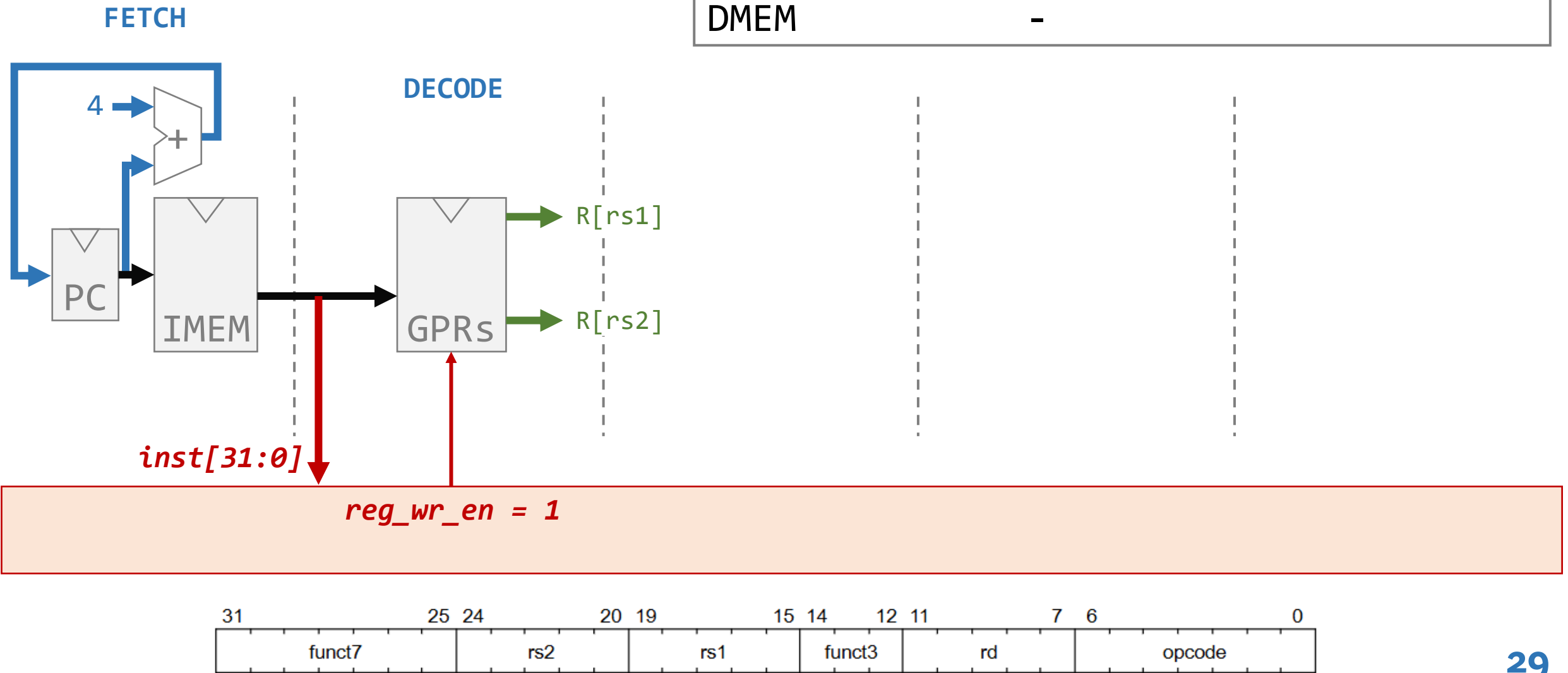
# Datapath for add

| State Element | Action                  |
|---------------|-------------------------|
| PC            | PC += 4                 |
| GPRs          | R[rd] = R[rs1] + R[rs2] |
| DMEM          | -                       |



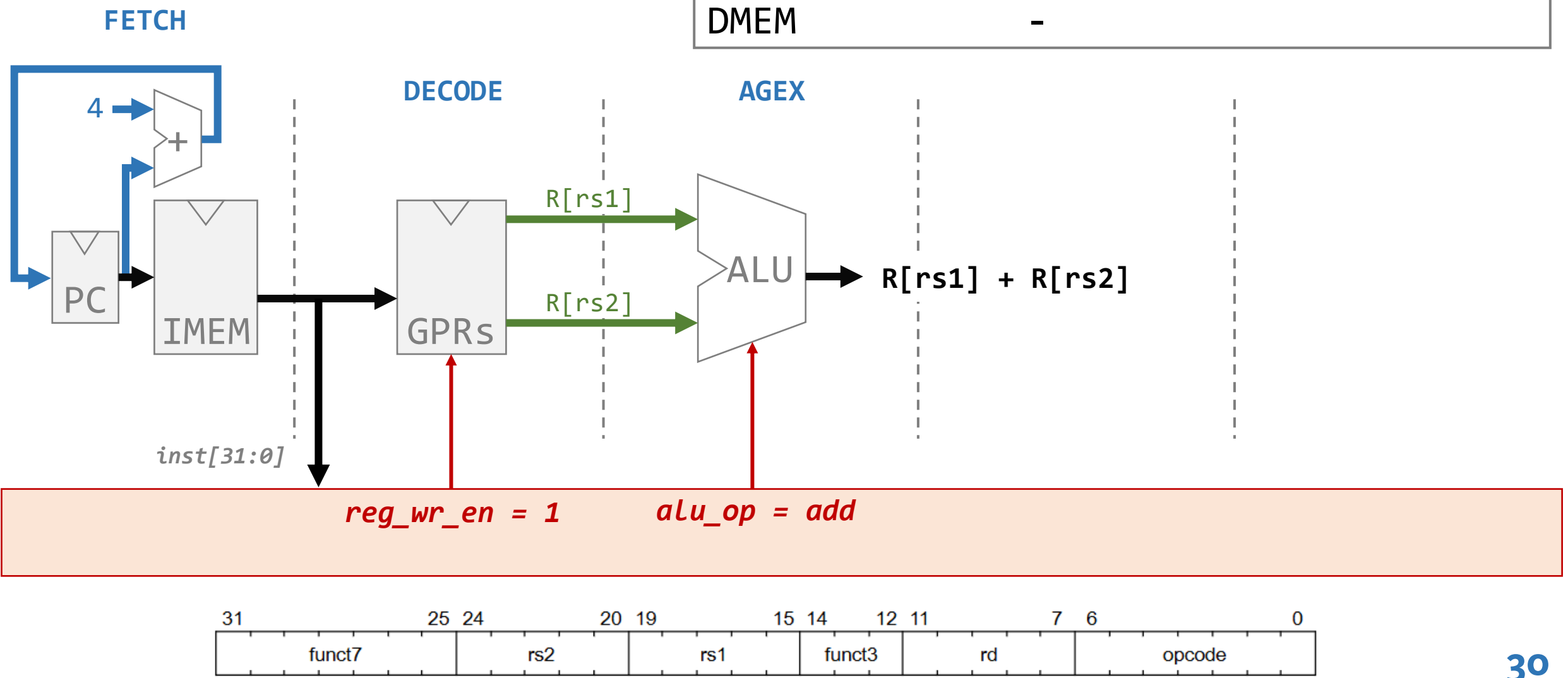
# Datapath for add

| State Element | Action                  |
|---------------|-------------------------|
| PC            | PC += 4                 |
| GPRs          | R[rd] = R[rs1] + R[rs2] |
| DMEM          | -                       |



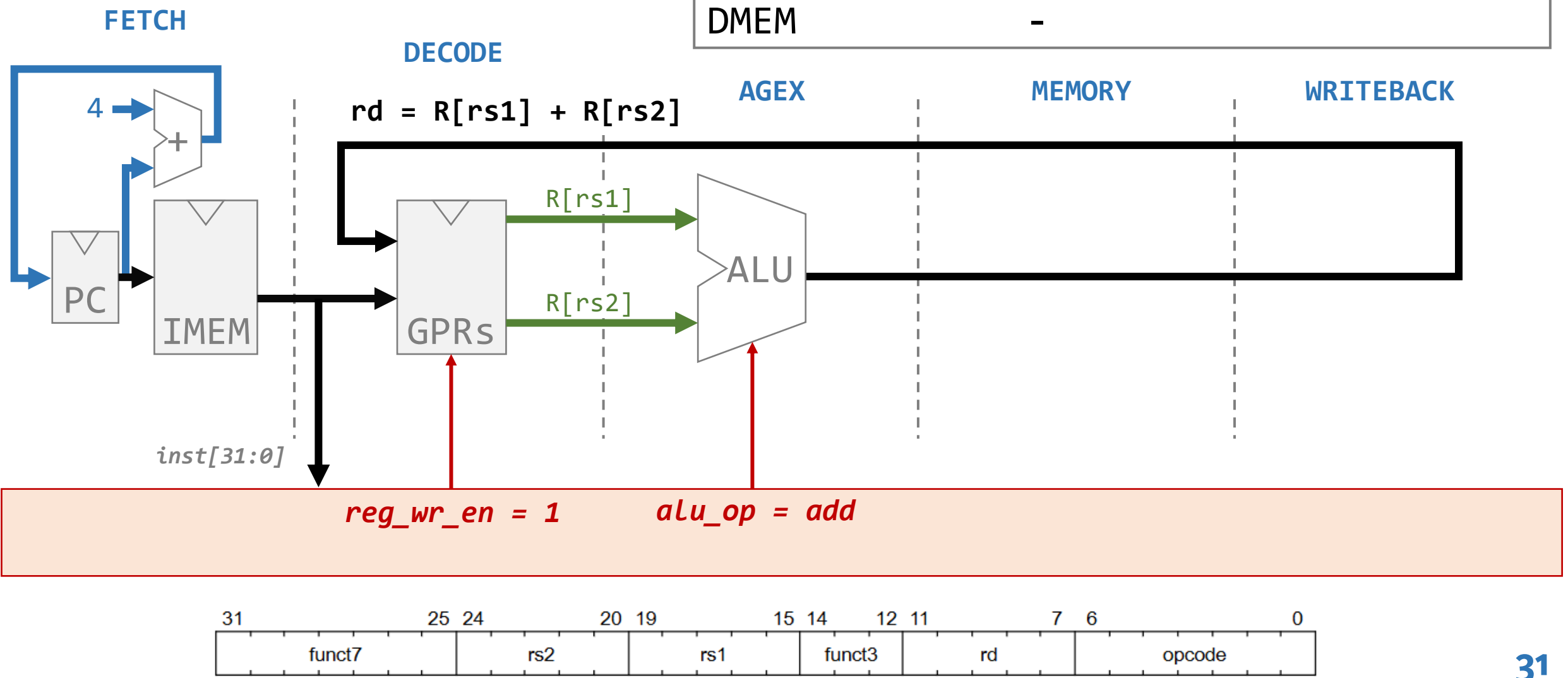
# Datapath for add

| State Element | Action                    |
|---------------|---------------------------|
| PC            | PC += 4                   |
| GPRs          | $R[rd] = R[rs1] + R[rs2]$ |
| DMEM          | -                         |



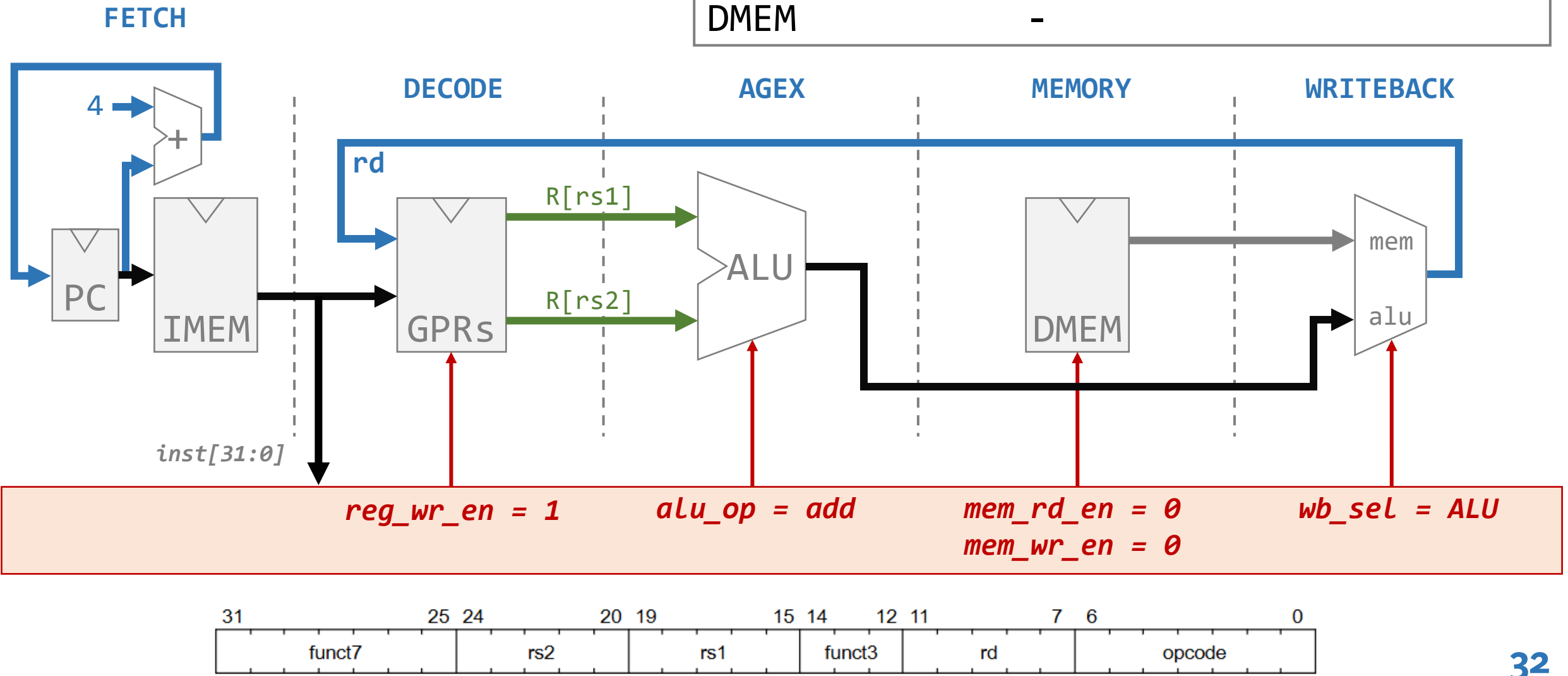
# Datapath for add

| State Element | Action                  |
|---------------|-------------------------|
| PC            | PC += 4                 |
| GPRs          | R[rd] = R[rs1] + R[rs2] |
| DMEM          | -                       |



# Datapath for add

| State Element | Action                  |
|---------------|-------------------------|
| PC            | PC += 4                 |
| GPRs          | R[rd] = R[rs1] + R[rs2] |
| DMEM          | -                       |



# Agenda

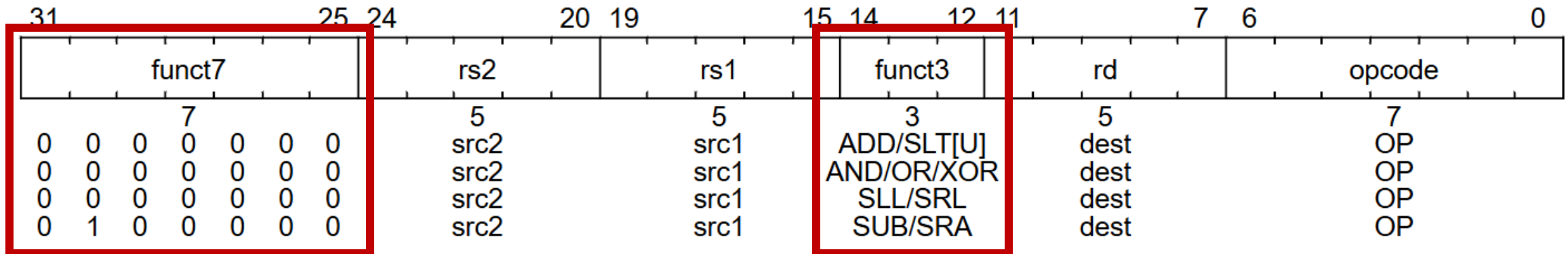
- Single-Cycle CPU
  - State Elements
- Five-Stage Execution Model
  - Implementing an ADD
  - **R-TYPE Instructions**
  - Any Instruction

# Extending the Datapath

- Would like to support **all RISC-V instructions**
- Much easier if we **group similar instructions**
  - Luckily, the ISA designers already did this for us

## R-TYPE (reg-reg)

<op> rd, rs1, rs2



- Control logic:
  1. Figures out this is an R-Type instruction
  2. Parses **funct3** and **funct7** to figure out the ALU operation

# Supporting All R-Type Instructions

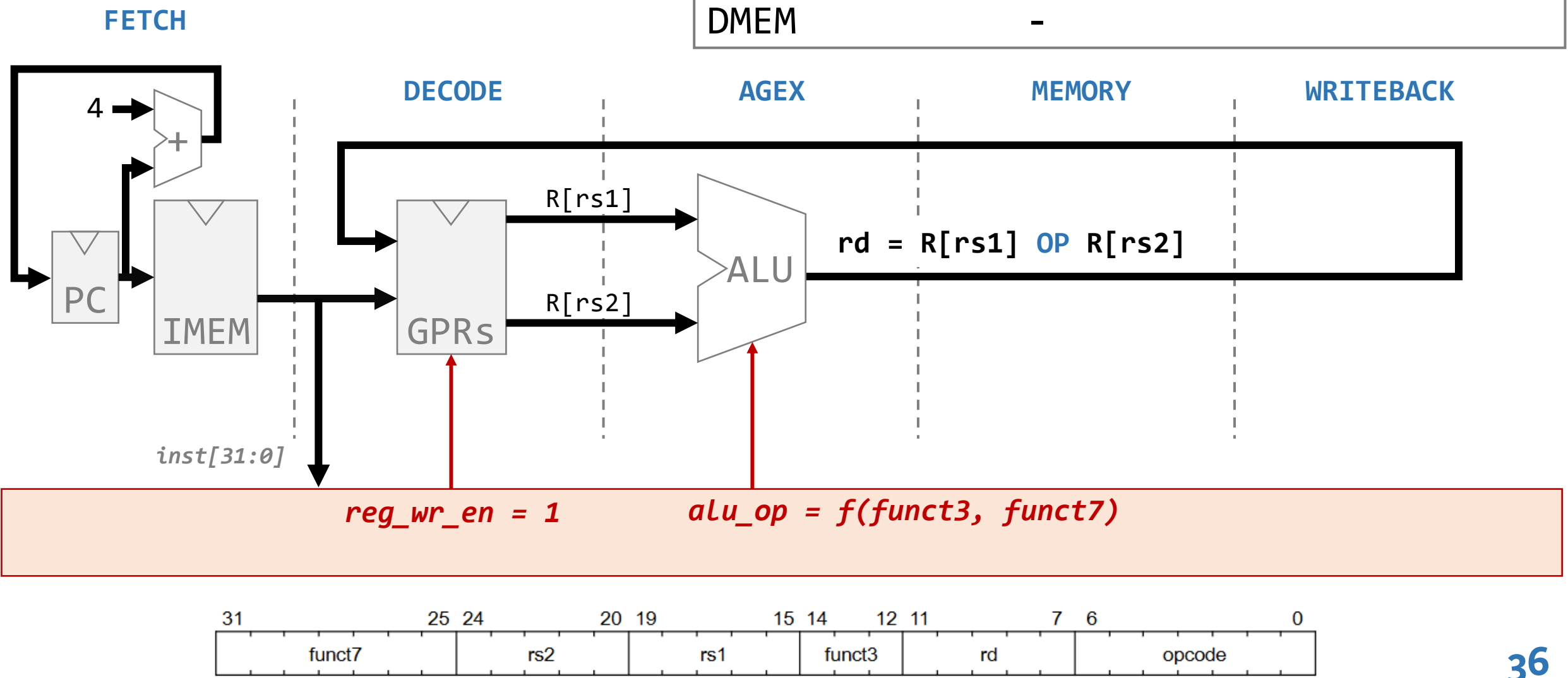
**<op>** rd, rs1, rs2

| funct7  |     |     | funct3 |    | opcode  | <op> |
|---------|-----|-----|--------|----|---------|------|
| 0000000 | rs2 | rs1 | 000    | rd | 0110011 | add  |
| 0100000 | rs2 | rs1 | 000    | rd | 0110011 | sub  |
| 0000000 | rs2 | rs1 | 001    | rd | 0110011 | sll  |
| 0000000 | rs2 | rs1 | 010    | rd | 0110011 | slt  |
| 0000000 | rs2 | rs1 | 011    | rd | 0110011 | sltu |
| 0000000 | rs2 | rs1 | 100    | rd | 0110011 | xor  |
| 0000000 | rs2 | rs1 | 101    | rd | 0110011 | srl  |
| 0100000 | rs2 | rs1 | 101    | rd | 0110011 | sra  |
| 0000000 | rs2 | rs1 | 110    | rd | 0110011 | or   |
| 0000000 | rs2 | rs1 | 111    | rd | 0110011 | and  |

**alu\_op = f(funct3, funct7)**

# R-TYPE Datapath

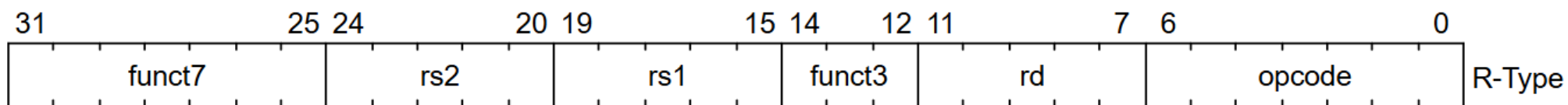
| State Element | Action                          |
|---------------|---------------------------------|
| PC            | PC += 4                         |
| GPRs          | R[rd] = R[rs1] <b>OP</b> R[rs2] |
| DMEM          | -                               |



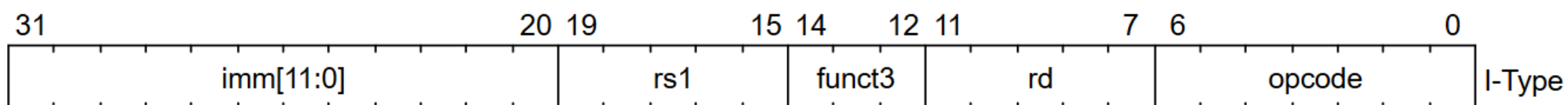
# Agenda

- Single-Cycle CPU
  - State Elements
- Five-Stage Execution Model
  - Implementing an ADD
  - R-TYPE Instructions
  - **Any Instruction**

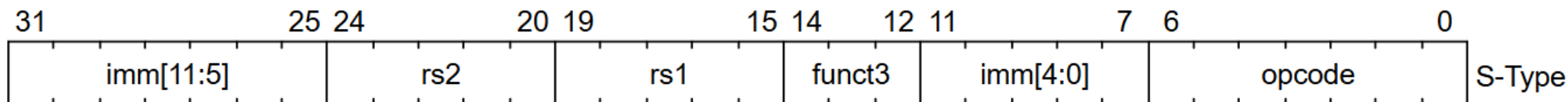
# 6 Types of RISC-V Instructions



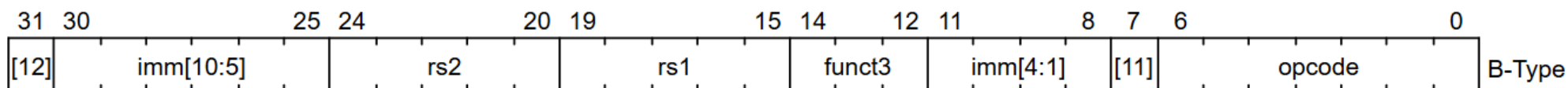
add, sub, slt(u),  
xor, or, and,  
sll, srl, sra



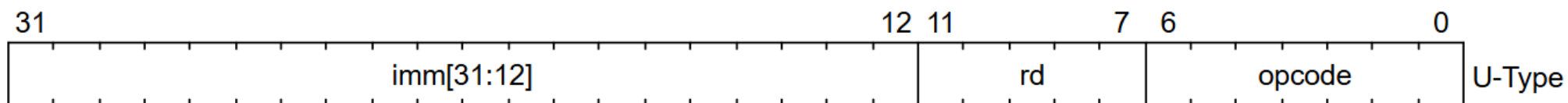
addi, subi, slt(u)i,  
xori, ori, andi, slli,  
srli, srai, lb(u),  
lh(u), lw(u), ld, jalr



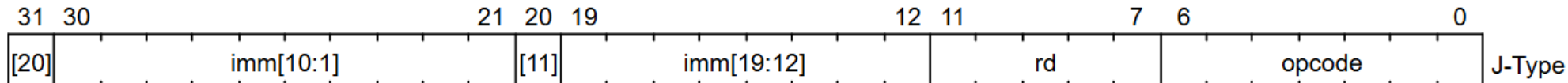
sb, sh, sw, sd



b<cond>



lui, auipc

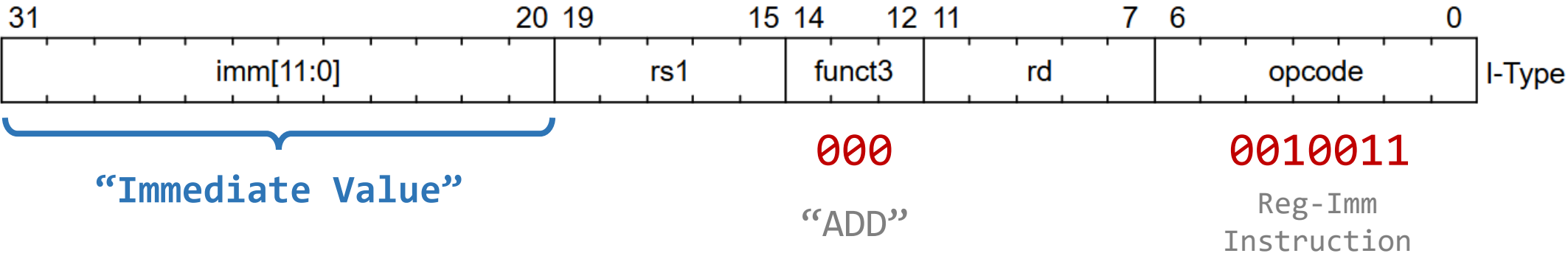


jal

# ADDI Instruction (I-Type)

- Similar to ADD, but **with an immediate value** instead

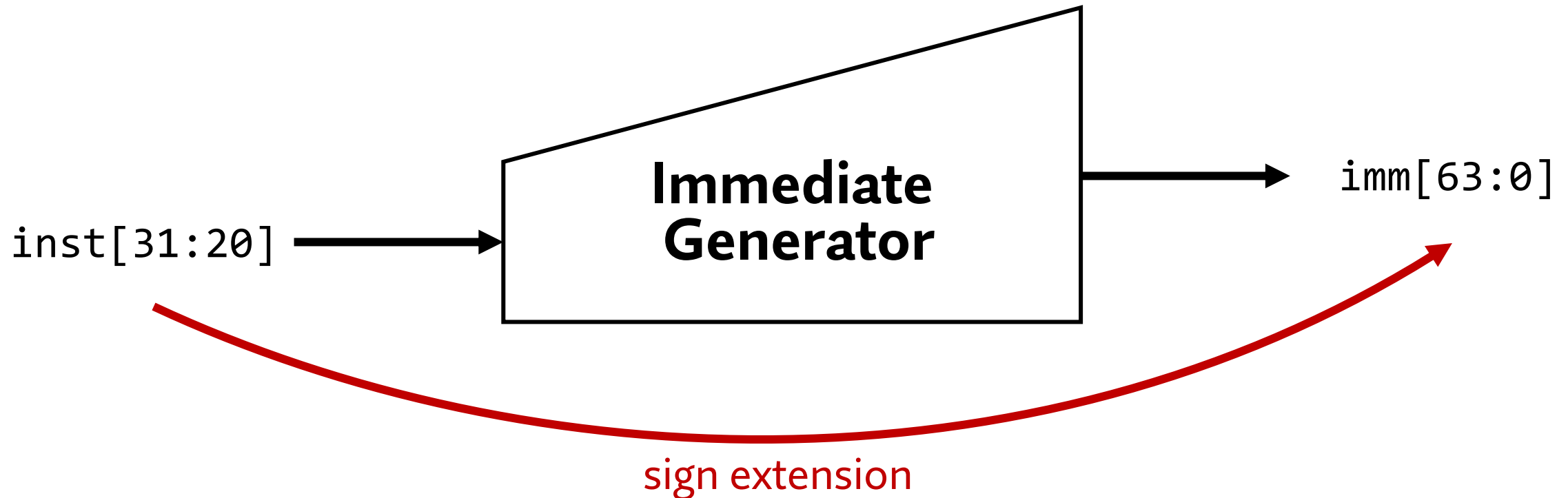
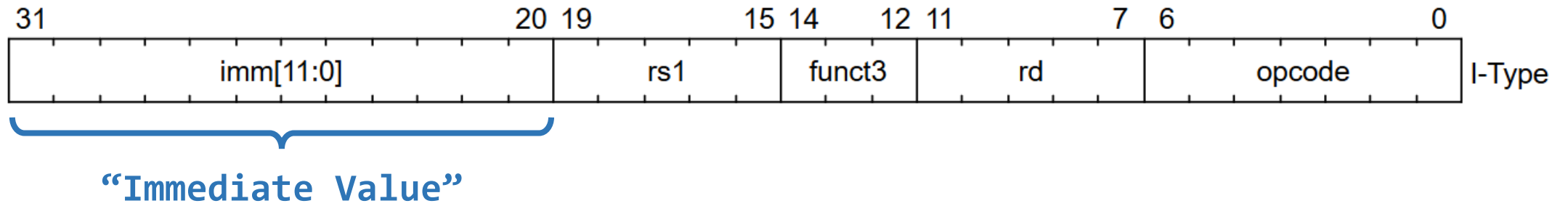
```
addi rd, rs1, imm
```



| State Element | Action                           |
|---------------|----------------------------------|
| PC            | PC += 4                          |
| GPRs          | R[rd] = R[rs1] + sext(imm[11:0]) |
| DMEM          | -                                |

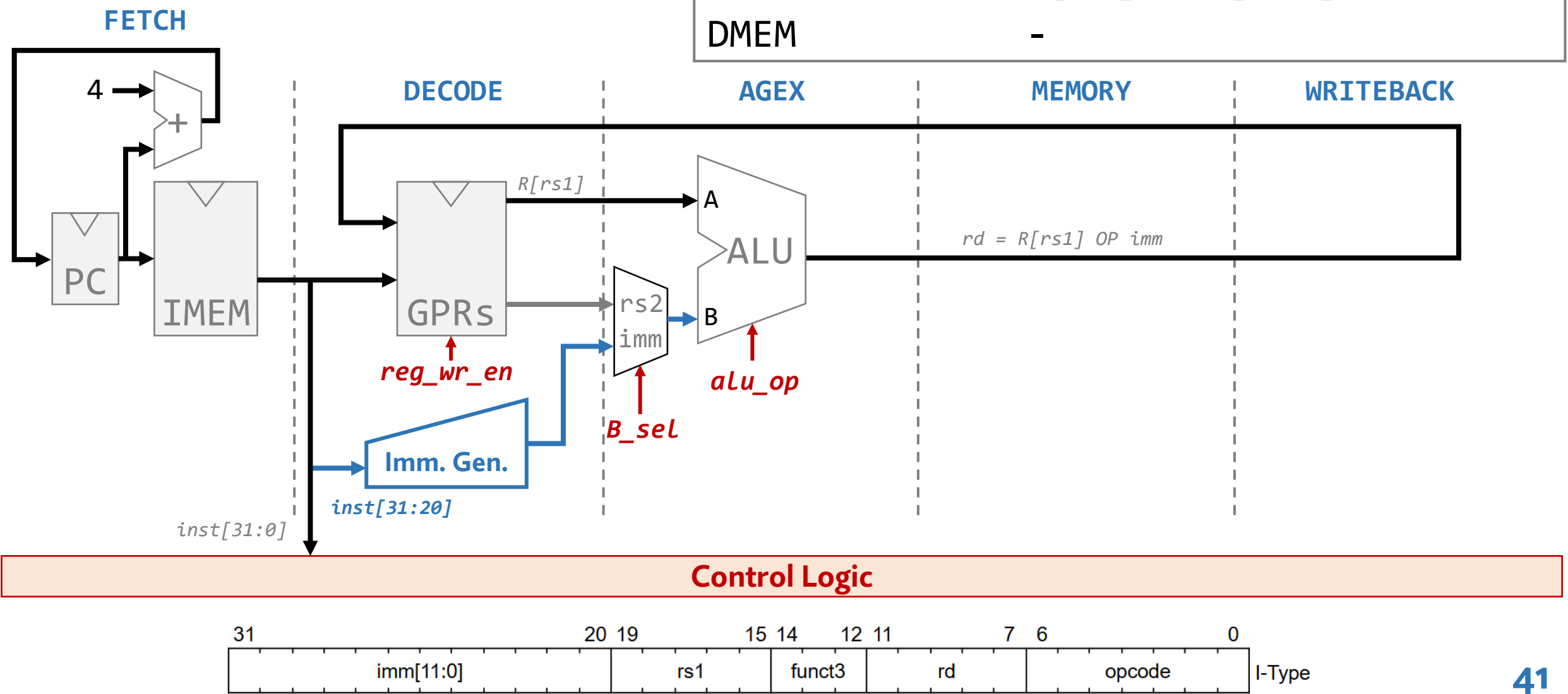
Need some logic block to generate imm

# Extracting an Immediate Value



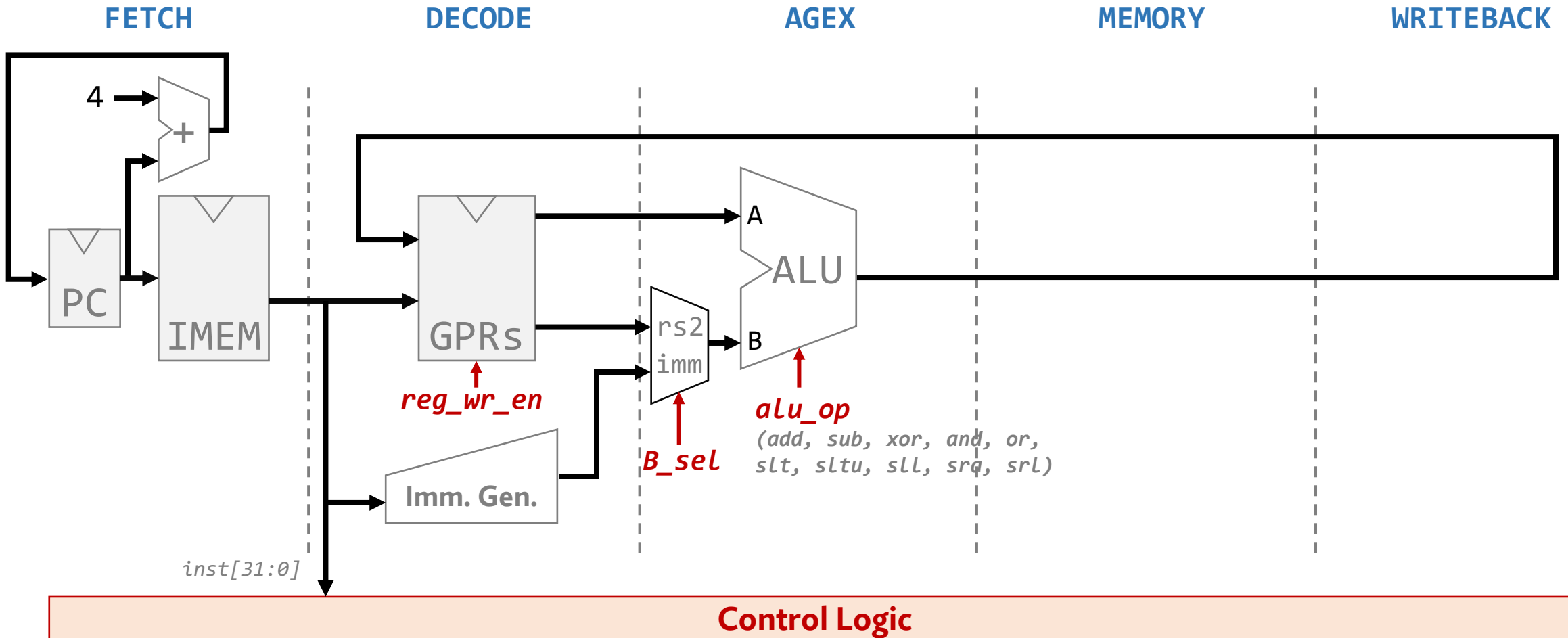
# I-TYPE Datapath

| State Element | Action                |
|---------------|-----------------------|
| PC            | PC += 4               |
| GPRs          | R[rd] = R[rs1] OP imm |
| DMEM          | -                     |



# Summary: Arithmetic/Logical Datapath

- **Datapath** propagates information
- **Control logic** chooses what to use vs. ignore



# **CS 211: Intro to Computer Architecture**

## ***12.1: Single-Cycle RV64I CPU - Arithmetic/Logic***

**Minesh Patel**

Spring 2025 – Tuesday 15 April